Methods that improve high frequency Single Flux Quantum electronics design

by

Paul le Roux

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Supervisor: Prof. C.J. Fourie

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Declaration

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This dissertation includes five original papers published in peer-reviewed journals or books and one unpublished publication. The development and writing of the papers (published and unpublished) were the principal responsibility of myself and, for each of the cases where this is not the case, a declaration is included in the dissertation indicating the nature and extent of the contributions of co-authors.

Date: March 2021

Abstract

Methods that improve high frequency Single Flux Quantum electronics design

P. le Roux

Department of Electronic Engineering,
University of Stellenbosch,
Private Bag X1, 7602 Matieland, South Africa.

Dissertation: Doctor of Philosophy

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In this thesis, we cover various methods that improve high-frequency Single Flux Quantum electronics design.

Accurately modelling high-frequency effects is vital in high-frequency Single Flux Quantum electronics design. The passive transmission line is, currently, the most inaccurately modelled circuit component. We, therefore, developed a new 2D quasi-Transverse-Magnetic method to calculate transmission line properties of superconductor structures. The new method can take into account quasi-particle losses as well as dielectric losses. The frequency response of a passive transmission line with arbitrary length can then readily be obtained from the transmission line properties.

The high-frequency response is informative, but a time-domain simulation model is necessary to determine the effect on high-frequency circuit dynamics. Accordingly, we developed the Superconductor Vector Fitting algorithm so that we can take arbitrary superconductor frequency responses and convert them into time-domain simulation models.

Complex dynamical behaviour, made more complicated by the new numerical simulation models, currently prohibits designing circuits by only using design equations. Automatic optimization routines are used to adjust circuit parameters to improve fabrication yield. Existing routines suffer from issues ranging from suboptimal circuits to severe performance issues. We developed a new and novel yield optimization algorithm, Distance-To-Failure-Maximization, that can be used to optimize superconductor circuits that are verified using time-domain simulations.

High-frequency circuits can be sensitive to changes in bias current from parasitics mutual inductances. We developed the fundamental inductance model to model all inductive effects accurately. The fundamental inductance model can also be used to construct design equations which accounts for parasitic effects as well as reduce the number of unknowns in the yield optimization procedure.

We use all the above methods in a detailed case study on the design of a JTLT. We take into account attenuation, impedance mismatch, flux mismatch, and resonance during the design of the JTLT circuit. With this, we conclude that the methods we developed have brought significant improvements to high-frequency Single Flux Quantum design.

Uittreksel

Metodes wat hoëfrekwensie ontwerp van Single Flux Quantum elektronika verbeter

(Methods that improve high frequency Single Flux Quantum electronics design)

P. le Roux

Departement Electronic Ingenieurswese,
Universiteit van Stellenbosch,
Privaatsak X1, 7602 Matieland, Suid Afrika.

Proefskrif: Doktor van Filosofie

Maart 2021

In hierdie tesis behandel ons verskillende metodes wat hoëfrekwensie ontwerp van *Single Flux Quantum* elektronika verbeter.

Akkurate modellering van hoëfrekwensie-effekte is uiters belangrik in 'n hoëfrekwensie *Single Flux Quantum* elektronika ontwerp. Die passiewe transmissielyn is tans die mees onakkuraatste gemodelleerde komponent. Daarom het ons 'n nuwe 2D kwasi-transvers-magnetiese metode ontwikkel om transmissielynseienskappe van supergeleierstrukture te bereken. Die nuwe metode kan kwasi-partikel-verliese sowel as diëlektriese verliese in ag neem. Die frekwensierespons van 'n passiewe transmissielyn met arbitrêre lengte kan dan maklik verkry word vanaf die transmissielynseienskappe.

Die hoëfrekwensie-respons is insiggewend, maar 'n tyd-domein-simulasiemodel is nodig om die effek op die hoëfrekwensie stroombaan dinamika te bepaal. Gevolglik het ons die *Superconductor Vector Fitting*-algoritme ontwikkel sodat ons arbitrêre frekwensie-response van supergeleiers kan neem en dit omskep in tyd-domein-simulasiemodelle.

Komplekse dinamiese gedrag, wat meer ingewikkeld gemaak word deur die nuwe numeriese simulasiemodelle, verbied tans die ontwerp van stroombane deur slegs ontwerp-vergelykings te gebruik. Outomatiese optimeringsroetines word gebruik om stroombaanparameters aan te pas om die vervaardigingsopbrengs te verbeter. Bestaande roetines ly van probleme wat wissel van suboptimale stroombane tot ernstige berekeningstyd probleme. Ons het 'n nuwe opbrengstoptimaliseringsalgoritme ontwikkel, *Distance-to-Failure-Maximization*, wat gebruik kan word om supergeleierstroombane te optimaliseer wat met behulp van tyddomein-simulasies geverifieer word.

Hoëfrekwensie-stroombane kan sensitief wees vir veranderinge in aanwendstroom wat veroorsaak word deur parasities magnetiese induktansies. Ons het die fundamentele induktansie-model ontwikkel om alle induktiewe effekte akkuraat te modelleer.

Die fundamentele induktansiemodel kan ook gebruik word om ontwerpvergelykings te konstrueer wat parasitiese effekte in ag neem, sowel as om die aantal onbekendes in die opbrengsoptimaliseringsprosedure te verminder.

Ons gebruik al die bogenoemde metodes in 'n gedetailleerde gevallestudie oor die ontwerp van 'n JTLT. Ons neem die attenuasie, die impedansie-wanaanpassing, die magnetiesevloed-wanaanpassing en die resonansie in ag tydens die ontwerp van die JTLT-stroombaan. Hiermee kom ons tot die gevolgtrekking dat die metodes wat ons ontwikkel het, 'n beduidende verbetering in die hoëfrekwensie-*Single Flux Quantum*-ontwerp gebring het.

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Chapter 1

Introduction

1.1 Motivation

Superconductor digital circuits are becoming larger and more complex in an effort to scale and improve superconductor circuits to challenge existing technologies. Superconductor digital electronics, such as Rapid Single Flux Quantum (RSFQ), can potentially offer improved power-efficiency, and increased performance over existing CMOS technologies. These Very Large Scale Integration (VLSI) efforts require robust and high-performance RSFQ logic cells that can operate at high frequencies. These RSFQ logic cells are used as building blocks that are assembled together to form complicated computation devices.

During the design of RSFQ logic cells, many simplifications and time consuming manual adjustments are made. These simplifications ease cell design and reduce design time, but impact the efficiency of the final cell. Manual modifications also tend to improve designs until the design is good enough or until the design time runs out. This results in suboptimal designs, which is not what is necessary for VLSI.

Any improvement to automated design optimization and simulation accuracy improves the cell designer's ability to design cells. Methods that improve high-frequency SFQ design are, therefore, essential to achieve VLSI.

1.2 Background on Superconductors

Superconductors are materials that starts exhibiting extraordinary behavior at low temperatures [1]. Superconductors expel magnetic field and have exactly zero DC electrical resistance [1]. The temperature at which a material becomes superconducting is known as the materials critical temperature, T_c. Superconductivity is a quantum mechanical phenomenon and superconductor's unique properties give rise to new and novel applications [1]. Superconductors can be used for low-noise sensors [2], particle detectors [3], fast and low power digital circuitry [4], high-quality resonators [5], and quantum computers [6].

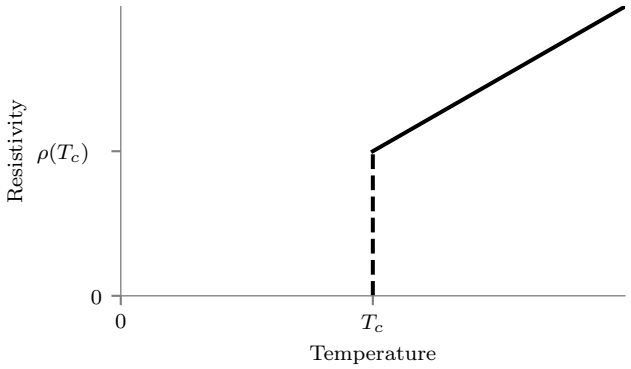

Figure 1.1: Visualization of the Resistivity vs Temperature of a superconductor

1.2.1 Discovery

Superconductivity was first observed, by Heike Kamerlingh Onnes, in 1911 [1]. He was investigating Mercury's resistivity at cryogenic temperatures [1]. He noticed the resistivity suddenly dropped to immeasurably small values below roughly 4.2 K [1]. Mercury has a critical temperature of approximately 4.2 K and the drop in resistivity that Onnes noticed was a result of the Mercury becoming superconductive [1].

Fig. 1.1 shows an illustration of the resistivity of a superconductor as it approaches absolute zero.

Critical current density and magnetic field

Onnes continued his cryogenic experiments, and in 1913 he discovered that materials lost it superconductor state if it was subjected to a strong enough current [1]. He also found that the current at which the superconductor loses its superconductivity is dependent on temperature [1]. This threshold current is today known as the critical current of a superconductor.

The next year, 1914, Onnes discovered that the superconductor could also lose its superconductivity as a result of a high applied magnetic field [1]. The threshold field at which the superconductor loses its superconductivity is also dependent on temperature [1]. This threshold magnetic field is today know as the critical field of a superconductor [1].

Meissner Effect

In 1933 Walther Meissner discovered that superconductors expel magnetic flux while in the superconducting state [1]. This is contrary to a perfect electric conductor which conserves the amount of flux inside it [1].

Fig. 1.2 shows an illustration of how the magnetic field gets expelled by the superconductors. The superconductor tries to minimize the magnetic flux inside the superconductor [1]. This leads to the expulsion of the magnetic field inside a superconductor [1]. A material that expels magnetic field is called a diamagnetic

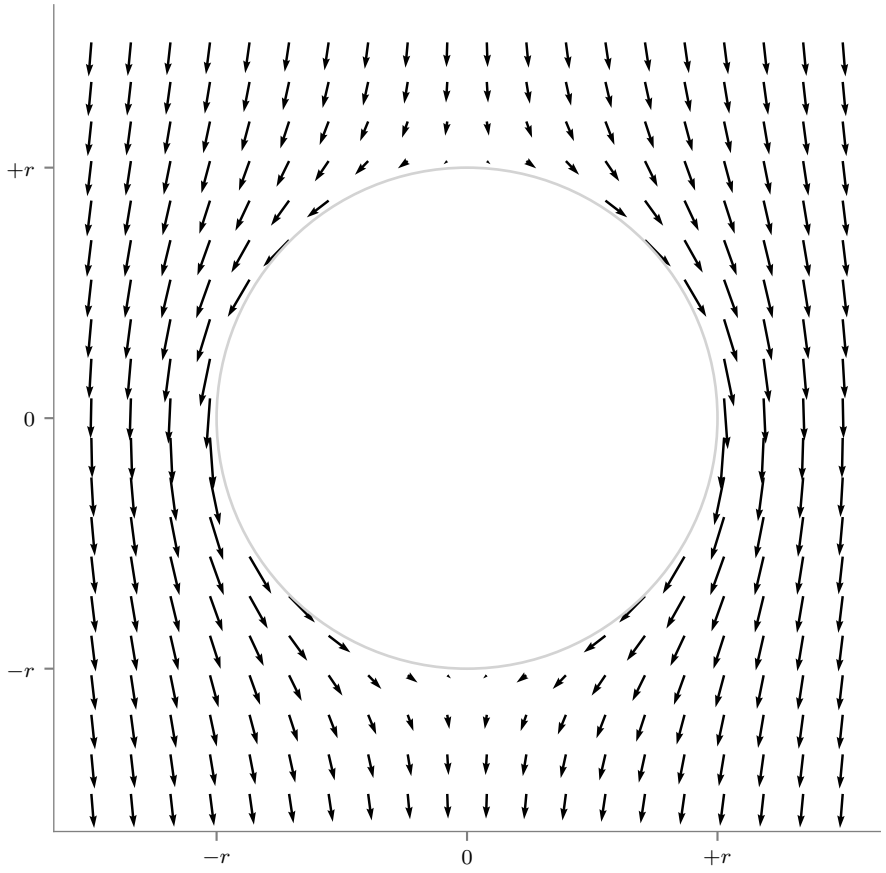

Figure 1.2: Visualization of the magnetic field in the presence of a large superconducting sphere

material [1]. In a superconductor, the ability to expel magnetic flux is called the Meissner effect [1]. This shown that superconductors are more than just perfect conductors [1].

1.2.2 London Equations

The first equations relating the superconductor current and electromagnetic field inside superconductors were developed two brothers, Fritz and Heinz London, in 1935 [7]. They did not prove the equations but provided logical arguments to show that the equations are plausible [7].

The brothers argued, similarly to others before them, that the electric field applies a force to the free moving electronics causing them to accelerate [7]. The first London equation is then

$$\mathbf{E} = \frac{\partial}{\partial t}(\Lambda \mathbf{J_s}), \tag{1.1}$$

where $\Lambda = \frac{m}{n_s e^2}$, n_s is a phenomological constant related to the density of superconductor electrons, m is the electron mass, e is the elctron charge, $\mathbf{E}$ is the electric field, and $\mathbf{J_s}$ is the super-current density.

They continued by taking the curl of the first London equation, (1.1), and applying Faraday's Law to obtain

$$\frac{\partial}{\partial t}\left(\mathbf{B} + \nabla \times (\Lambda \mathbf{J_s})\right) = 0, \tag{1.2}$$

where $\mathbf{B}$ is the magnetic field.

From the Meissner effect they knew that the constant, but non-zero solutions of (1.2), where non-physical [7]. They concluded that the inner expression must be zero [7]. The second London equation is therefore

$$\mathbf{B} = -\nabla \times (\Lambda \mathbf{J_s}). \tag{1.3}$$

The two equations, (1.1) and (1.3), describe the fields inside a superconductor and are known as the London equations.

London penetration depth

Combining Amperes Law and the second London equation one can derive

$$\nabla^2 \mathbf{B} - \frac{\mu_0}{\Lambda}\mathbf{B} = 0, \tag{1.4}$$

where μ_0 is the permeability of free space.

Equation (1.4) describes a lossless conductor with a penetration depth of λ, where

$$\lambda = \sqrt{\frac{\Lambda}{\mu_0}}. \tag{1.5}$$

λ, from (1.5), is known as the London penetration depth. The magnetic field from outside the superconductor decays at a rate of $e^{-\lambda}$ per meter inside the superconductor.

In a bulk superconductor, 63.2% of the magnetic field is contained within one London penetration depth, and 95.0% is contained within three London penetration depths. As the superconductor bulk increases in size, the superconductor centre contains negligible current and magnetic field resulting from the expulsion of the magnetic field.

Fig. 1.3 illustrates the case where the width of the superconductor, a, is significantly larger than the London penetration depth. Current flows close to the surface of the superconductor to counteract the magnetic field applied to the superconductor. The centre of the superconductor then contains negligible amounts of current and field.

Fig. 1.4 illustrates the case where the width of the superconductor, a, is significantly smaller than the London penetration depth. The magnetic field still penetrates the superconductor but does not get expelled as in the bulk limit.

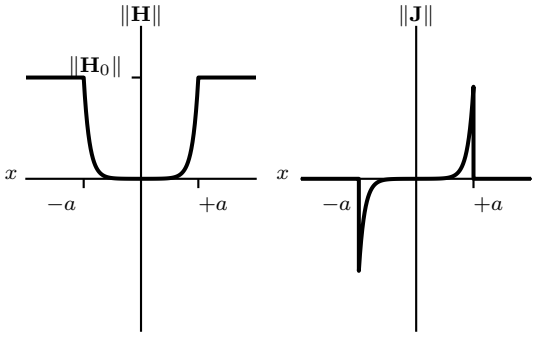

Figure 1.3: Visualization of the magnetic field penetration and current density in the bulk limit in superconductors

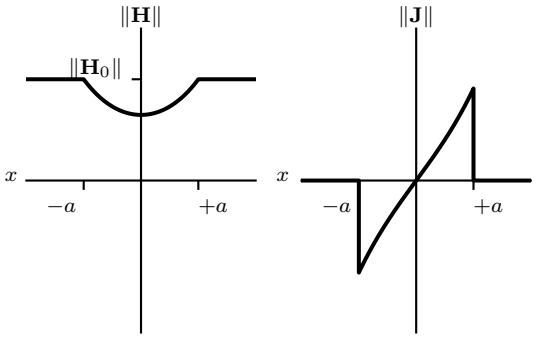

Figure 1.4: Visualization of the magnetic field penetration and current density in a thin film superconductors

1.2.3 Macroscopic Quantum Model

The London equations well describe superconductors, but the London equations are not a comprehensive description of the superconducting effect. The superconducting phenomenon is a macroscopic quantum effect, and by 1948 the London brothers were able to show that they could derive their equations from Schrodinger's equation. Schrodinger's equation,

$$i\hbar\frac{\partial}{\partial t}\Psi = -\frac{\hbar^2}{2m}\nabla^2\Psi + V\Psi, \tag{1.6}$$

describes a probability amplitude of particles where Ψ is the probability density of the particles, V is the potential energy operator, and $\hbar$ is the reduced Planck constant. The density of the probability amplitude describes the super electron density, n_s.

$$|\Psi| = \Psi^*\Psi = n_s \tag{1.7}$$

For simplicity, it is assumed that the super electron density is constant. The integral over the total volume is then also equal to the total number of super-electrons, N_s.

$$\int \Psi^*\Psi dv = N_s \tag{1.8}$$

The probability amplitude is necessarily complex and can be written as

$$\Psi = \sqrt{n_s}e^{i\theta} \tag{1.9}$$

where θ is the phase of the wave function.

By using the Lorentz force law, we can derive the equation of the superconductor current

$$\Lambda \mathbf{J_s} = -\mathbf{A} + \frac{\hbar}{q}\nabla\theta, \tag{1.10}$$

where q is the charge density.

This equation is called the supercurrent equation. Taking the curl of (1.10) results in (1.3). By taking the time derivative of (1.10) and manipulating we arrive at

$$\mathbf{E} = \frac{\partial}{\partial t}(\Lambda \mathbf{J_s}) + \frac{1}{nq}\nabla\left(\frac{1}{2}\Lambda {\mathbf{J_s}}^2\right). \tag{1.11}$$

It is clear that (1.11) is more than the first London equation (1.1). It can be shown that the London brothers did not take into account the full Lorentz force, and inadvertently assumed that the current is not affected by the magnetic field. Since superconductors break under strong magnetic fields and superconductors minimize their internal magnetic field, the assumption is plausible in the general case. In the study of superconductor low-power electronics, the assumption is considered valid.

1.2.4 Quantization of Magnetic Flux

If we take a contour integral of (1.10) over a contour C we get

$$\oint_C \Lambda \mathbf{J_s} \cdot d\mathbf{l} = -\oint_C \mathbf{A} \cdot d\mathbf{l} + \oint_C \frac{\hbar}{q}\nabla\theta \cdot d\mathbf{l}, \tag{1.12}$$

which simplifies to

$$\oint_C \Lambda \mathbf{J_s} \cdot d\mathbf{l} + \int_S \mathbf{B} \cdot d\mathbf{s} = \frac{\hbar}{q}2\pi n, \tag{1.13}$$

where $n \in \mathbb{Z}$.

From (1.13) it can be seen that the magnetic flux in a superconductor is quantized. We can then define a fluxon, $\Phi = \frac{\hbar 2\pi}{q}$, as the unit of quantized flux.

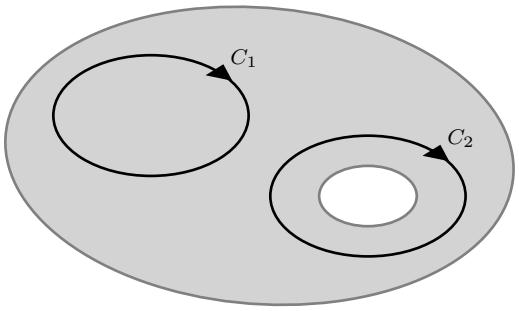

Figure 1.5: Illustration of different contour integral lines in a superconductor

The quantization can be divided into two cases. The first case where the contour forms a simply connected region and the second case where it does not. Fig. 1.5 illustrates the two cases as C_1, and C_2 respectively. In the simply connected case, the contour can be reduced in size until the left-hand side of (1.13) becomes zero. Therefore, in the simply connected case $n = 0$. However, if the contour does not form a simply connected region, then the integrals do not need to be zero, and n is not necessarily zero.

The superconductor, therefore, traps flux in quantized units in holes in the superconducting structure. The trapped flux cannot be moved out of the hole without partially breaking the superconductivity, or tunnelling through a superconducting area.

1.2.5 Josephson Junction

The superconductor wave function, being a quantum wave function, can extend past the extents of the superconductor [1]. When two superconductors are separated by a thin potential barrier, such as an insulator, the super-electrons can tunnel through the potential barrier. This is known as the Josephson effect. A visualization of the wave function across an insulating barrier is shown in Fig. 1.6. The device formed by the Josephson effect is called a Josephson Junction.

For a small Josephson junction, the relationship between the phase of the two wave functions and the current across the Josephson junction is given by Equation (1.14).

$$I_J = I_C \sin(\phi_1 - \phi_2), \tag{1.14}$$

The current through the junction is I_J, and I_C is the junctions critical current. The phase of the wave functions on the boundaries of the insulator are ϕ_1 and ϕ_2. If the current exceeds the junctions critical current, the dominant transport mechanism becomes normal electron tunnelling rather than super-electron tunnelling.

The two superconductor plates also act as a capacitor at non-zero frequencies.

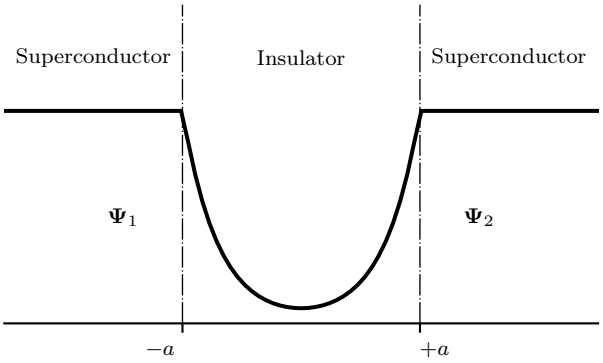

Figure 1.6: Illustration of the superconductor wave function across a barrier

Taking the current-phase relationship, non-linear normal electron tunnelling, and capacitive effect into account an approximate lumped circuit element representation, known as the RSCJ model, can be constructed. The RSCJ model circuit equivalent is shown in Fig. 1.7.

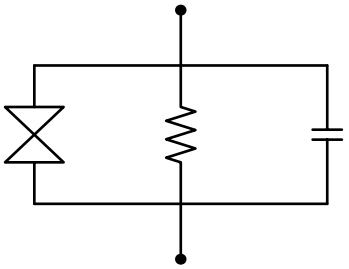

Figure 1.7: Generalized RCSJ circuit model

The hourglass element in Fig. 1.7 denotes the super-current phase relationship. The Josephson Junction as a whole is often denoted by the more compact cross, as shown in Fig. 1.8.

The DC IV-characteristics of the Josephson Junction can be hysteretic. The Stewart-McCumber parameter, β_C, of the junction, as given by Equation (1.15), denotes the ratio of the RC-time constant and the Junction time-constant.

$$\beta_C = \frac{2\pi}{\Phi_0} I_C R_J^2 C_J, \tag{1.15}$$

where R_J is the junction's resistance and C_J is the junction's capacitance.

If the junction is over-damped, $\beta_C > 1$, then the RC-time constant dominates the response time, and the junction is non-hysteretic. If the junction is under-damped,

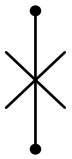

Figure 1.8: Josephson Junction Circuit Component Diagram

$\beta_C < 1$, then the Junction time constant dominates the response time and the junction is hysteretic. For minimal response time, the junction needs to be critically damped, $\beta_C = 1$.

The Stewart-McCumber parameter can be engineered by adding a shunt resistor in parallel to the junction. It is common in literature for the shunt resistor to be left out of the circuit diagram and only to state the designed Stewart-McCumber parameter.

The exact junction response is, unfortunately, much more complicated as the external circuitry and the junction non-linearity influences the response. Even if the junction is viewed in isolation with its shunt resistor the shunt resistor has an inductance which causes the response to change in a non-negligible way. This makes it essential to perform dynamic simulations to verify superconductor circuit behaviour.

1.3 Background on Single Flux Quantum Electronics

There are multiple types of digital superconductor electronics. Single Flux Quantum (SFQ) [4; 8; 9; 10; 11], Quantum Flux Parametron (QFP) [12; 13], Reciprocal Quantum Logic (RQL) [14], are all superconductor electronics families with different advantages and disadvantages. We will focus on Single Flux Quantum (SFQ) as it is the oldest and most researched superconductor electronic technology still in development today. Types of SFQ technologies include Rapid SFQ (RSFQ) [4], LR-loaded RSFQ (LR-RSFQ) [8], Low Voltage RSFQ (LV-RSFQ) [9], Energy-Efficient RSFQ (ERSFQ) [10], and Efficient SFQ (eSFQ) [11]. We will further refine our focus on RSFQ for its reliability and extensive research.

1.3.1 Logic

If a Josephson Junction is driven with a current that exceeds its critical current, the Josephson Junction lets through an integer number of magnetic flux quanta or, differently stated, an integer number of single flux quantum passes through the junction [4]. If only one single flux quantum passes the junction, the result is a picosecond scale voltage pulse [4]. This pulse has an area of one Φ_0 [4].

$$\int V_{SFQ}(t)\ dt = \Phi_0, \tag{1.16}$$

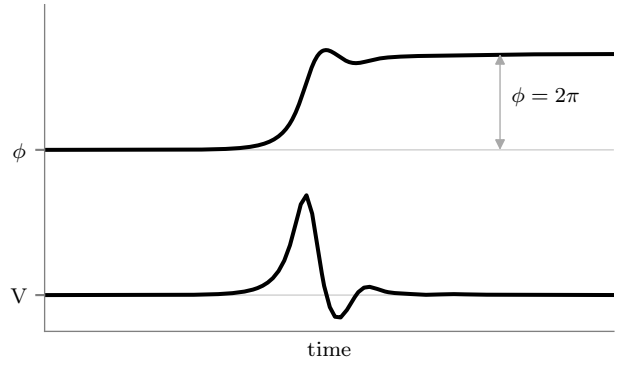

Figure 1.9: Single Flux Quantum Pulse

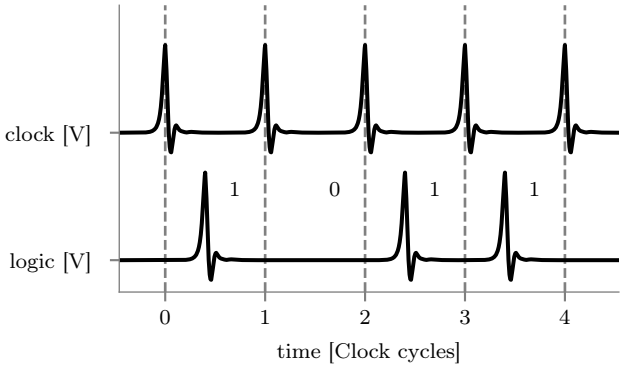

Figure 1.10: Single Flux Quantum Logic

where $V_{SFQ}(t)$ is the voltgae of an SFQ pulse.

Since the relationship between current and phase is $\frac{d\phi}{dt} = \frac{2\pi}{\Phi_0}V$, the pulse is also equivalent to a 2π phase shift [4]. A SFQ pulse and its phase shift is visualized in Fig. 1.9.

The short time scale and quantized area of the pulse make it ideal for digital circuits [4]. These pulses can be used to encode digital information [4]. RSFQ circuits encode a digital one as the presence of a pulse and encode a digital zero as the absence of a pulse [4]. This encoding requires synchronization with a reference clock pulse to disambiguate a late pulse from an absent pulse [4]. Fig. 1.10 illustrates the logic encoding.

1.3.2 Transmission

If a junction undergoes a 2π phase shift, the phase difference causes a redistribution of current in the circuit [4]. If a receiving junction is current-biased, the additional

current that enters it can cause it to trigger and create another SFQ pulse [4]. This is the idea behind the Josephson Transmission Line (JTL), which carries the pulse forward [4].

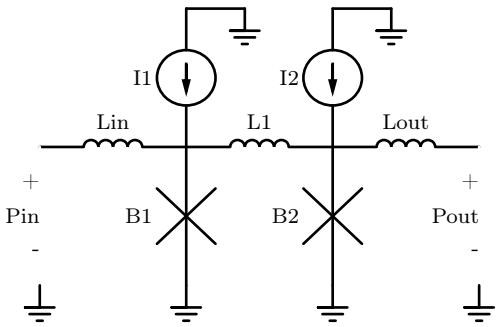

Figure 1.11: Josephson Transmission Line Circuit Schematic

Fig. 1.11 shows a JTL circuit. The junctions are biased so that they will trigger after the previous junction has triggered [4]. This causes the pulse to propagate along the JTL [4].

The JTL has very high operating margins [15]. It can be used as an impedance matching circuit between other cells and can also be used to introduce an additional time delay [15; 16].

1.3.3 Storage and Decision

Since a pulse redistributes current, a pulse can cause a superconductor circuit to store flux or release stored flux from the circuit [17]. If a junction in a JTL does not provide enough current to trigger the next junction flux is stored in the loop between the two junctions [4]. The stored flux acts as a new current bias in the circuit [4]. If another junction is attached to the untriggered junction, it can be used as a Decision-Making Pair (DMP) [18].

Fig. 1.12 shows an RSFQ D-Flip Flop (DFF), which operates on this principle. If there is flux is stored between junction B1 and B2, then an arriving clock pulse will cause B2 to trigger and release an output pulse [4]. If there is no flux stored between junction B1 and B2, then an arriving clock pulse will cause B3 to trigger without releasing an output pulse [4].

1.3.4 Buffer

Backward current in the circuit might cause a junction to undergo a 2π phase shift and result in a pulse being transmitted in the backward direction on transmission

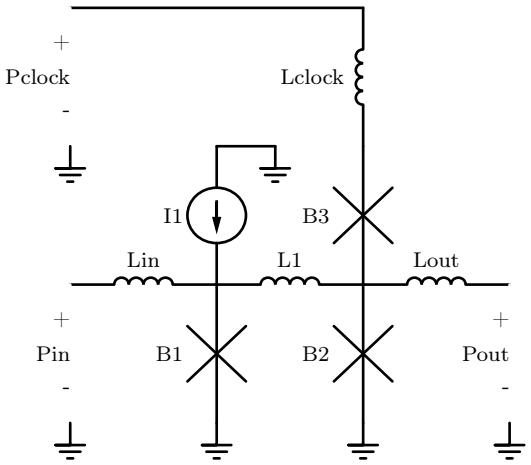

Figure 1.12: Single Flux Quantum DFF Circuit Schematic

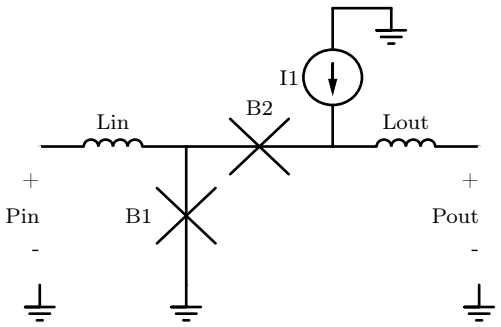

Figure 1.13: Single Flux Quantum Buffer Circuit Schematic

elements [19]. This is not the desired behaviour and will potentially break the operation of other components if a pulse arrives from an output port [4; 19]. An escape junction can be used to release a reverse pulse [4; 19].

Fig. 1.13 shows a buffer circuit using an escape junction, B2. An input pulse will trigger B1 and transmit an output pulse [4]. A pulse from the output will trigger B2 and leave the circuit [4].

1.3.5 Logic gates

The operation of an SFQ logic gate follows a pattern [17]:

1. An inputs pulse arrives

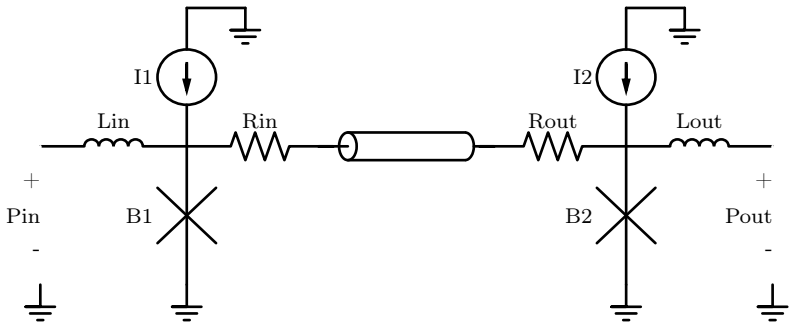

Figure 1.14: Single Flux Quantum Passive Transmission Line Driver and Reciever Circuit Schematic

2. Flux is possibly stored, moved, or released
3. Possible transmission of output pulses

This pattern can be implemented using a combination of multiple transmission, storage, decision, or buffer parts [18]. Decomposing a circuit into these basic structures simplifies the understanding of the circuit. The biasing point of the circuit has to be adjusted to maintain the correct operation.

The bias current can be applied in any manner as long as the junctions are biased with the correct currents. Current sources can be moved, and current can flow between parts of the circuit. Bias current can also be applied with flux linkage, as is sometimes the case in eSFQ [11].

1.3.6 Passive Transmission line

The distance between logic gates increases as designs become larger [20]. One cannot increase the distance between junctions in a JTL indefinitely as the flux could potentially become stored if the inductance in the connecting loop becomes too large [21]. Chaining JTLs together requires a large amount of biasing current, and introduces a considerable time delay [20]. By adding a resistive element in series in the loop prevents flux from being trapped and the pulse can then ballistically propagate along the line [20].

Fig. 1.14 shows a passive transmission line driver and receiver circuit, which can be used to connect gates between long distances.

1.4 Objectives

With the ever-increasing importance of cell design in superconductor VLSIs, we aim to develop more accurate, faster, and more robust methods to aid circuit designers. In effect, we are improving electronic design automation (EDA) for high-frequency SFQ circuits.

Our developed methods aim to improve modelling accuracy, simulation integration, and automated circuit optimization. All methods address problems faced by circuit designers today.

We have summarized the objectives of this dissertation by specifying the areas we intend to improve:

1. High-frequency characterization of superconductor transmission line structures
2. Accurate high-frequency superconductor SPICE models
3. Improved automated yield optimization of RSFQ circuits
4. Improved inductance modelling

1.5 Document Layout

In Chapter 2, published work on high-frequency passive transmission lines is presented. The contributions of this work and the importance of the contributions to this dissertation are highlighted.

In Chapter 3, superconductor vector fitting is presented to produce a superconductor state-space macro model from a frequency-response. The required theory behind modelling and vector-fitting is presented. How the vector fitting technique is extended to superconductor models is explained. The Passive Transmission Line is handled in detail, and a highly accurate SPICE model is produced.

In Chapter 4, published work on the Distance-to-Failure-Maximization optimization algorithm for RSFQ cells is presented. The contributions of this work and the importance of the contributions to this dissertation are highlighted.

In Chapter 5, work submitted for publication on the fundamental inductance model is presented. The contributions of this work and the importance of the contributions to this dissertation are highlighted.

In Chapter 6, the cumulative work in this thesis is applied to the design of a Josephson Transmission Line with integrated drivers and receivers (JTLT). The JTLT is designed to function at high frequency, 100 GHz, and even when driving a PTL at resonance. The high-frequency PTL SPICE model is used to account for pulse transmission and reflection in the circuit accurately. The JTLT is optimized for fabrication yield using the DFM algorithm.

Chapter 2

PTL frequency-domain modelling

2.1 Introduction

The distance that single flux quantum (SFQ) pulses need to be transmitted continuously increases as more complicated designs increase chip area. Very-large-scale integration (VLSI) requires automated place-and-route tools [22], and these tools could create long routes between connected components. Superconducting passive transmission lines (PTLs) are used to transmit SFQ pulses across these long distances [23]. Dispersion and attenuation on the PTL can lead to timing variations and even operational failure.

Modelling a PTL as an ideal lossless transmission line [20; 23] ignores AC-losses in the superconductors. Linearizing the superconductivity effect at the point where the SFQ pulse train carries maximum energy is more accurate [20], but it then incorrectly includes DC losses. Flux trapping cannot happen in a loop with DC losses, and this fundamental phenomenon is, therefore, not included in the model. Thus, for accurate designs of long-distance interconnects an improved superconductor passive transmission line model is required.

In this chapter, we develop a numerical method to calculate the frequency-dependent characteristics of superconductor transmission line structures efficiently. The ambient temperature and changes in penetration depth with frequency are taken into account when solving the electromagnetic fields of a superconductor transmission line. The frequency-dependent effects of an example PTL designed for the MIT-LL SFQ5ee process [24] are shown.

2.2 Published Work

All relevant work, attached in Appendix A, is published in

- P. le Roux, K. Jackman, J. A. Delport, and C. J. Fourie, "**Modeling of Superconducting Passive Transmission Lines**," IEEE Trans. Appl. Supercond., vol. 29, no. 5, pp. 1-5, Aug. 2019.

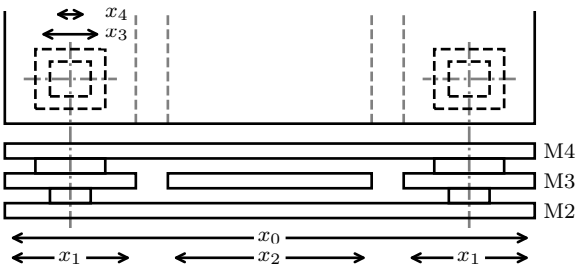

Figure 2.1: PTL illustration with the accentuated features for visibility. The image originally appeared in the article as attached in Appendix A.

2.3 Summary of research contribution

- The numerical instability noted in the numerical calculation of Zimmermann's superconductor complex conductivity [25] was fixed.
- The singularities in Zimmerman's superconductor complex conductivity integral [25; 26] was analytically removed by using the Gauss-Chebyshev quadrature to perform the integral. This resulted in improved accuracy and improved the efficiency of numerical routine.
- The quasi-TM formulation [27] was transformed into weak-variational form. FEniCS [28], a FEM library, was used to solve the weak-variational form. This resulted in a numerical programme that can calculate the transmission line properties of a given transmission line structure.

2.4 PTL example

As an example, we will, throughout this thesis, use a 4.5 µm wide PTL designed for the MIT-LL SFQ5ee process. The width was chosen to give a DC characteristic impedance, Z_0, of approximately 5 Ω. The dimensions and parameters are the same as given in Appendix A.

Fig. 2.1 shows an illustration of the example PTL. All layers have a thickness of 200 nm, and $x_0 = 9.1$ µm, $x_1 = 1.8$ µm, $x_2 = 4.5$ µm, $x_3 = 1.2$ µm, and $x_4 = 0.6$ µm The ground-plane and sky-plane, of the MIT-LL PTL, are continuously stitched with a stitch pitch of 5 µm. In this thesis, we will ignore the 3D effects as they have negligible influence on the propagation parameters.

The material parameters for Niobium are listed in Table 2.1, and are the same as in Appendix A. Data on the dielectric losses over frequency in the SFQ5ee process were unavailable, so a lossless dielectric with $\epsilon = 4.6\epsilon_0$, where ϵ_0 is the permittivity of free space, was used.

The quasi-TM FEM solver, along with Zimmerman's superconductor complex conductivity, was used to determine the accurate characteristic impedance and prop-

Parameter	Value
Δ_0	$1.5\,\mathrm{meV}$
$\frac{\lambda_0}{\xi_0}$	2.3
σ_{dc}	$2.4 \times 10^5\,\mathrm{S\,cm^{-1}}$
$\tau_{scatter}$	$3 \times 10^{-14}\,\mathrm{s}$

Table 2.1: Niobium material parameters

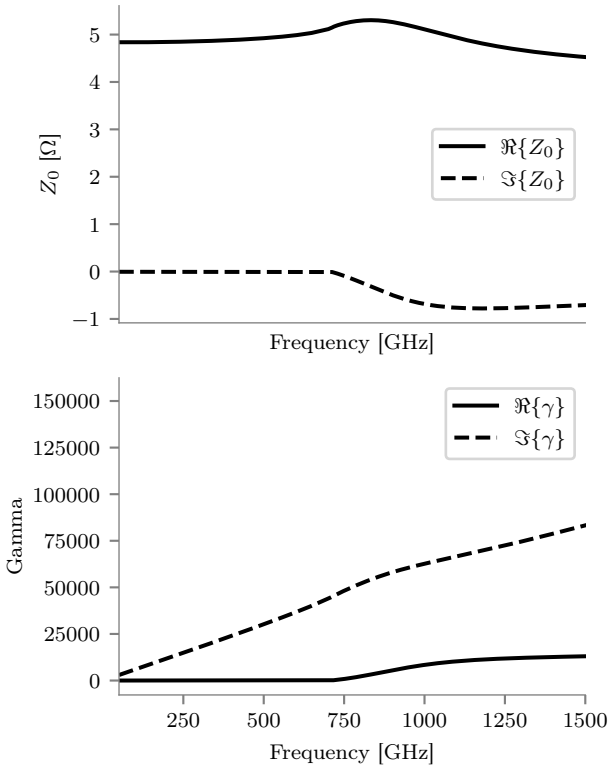

Figure 2.2: Frequency dependent per-unit parameters of the PTL under study

agation constant of the example PTL. The temperature, as in Appendix A, was set to 4 K. The results are shown in Fig. 2.2.

2.5 Conclusion

The numerical method to calculate complex conductance expression from Zimmermann was improved. A technique that can be used to determine the propagation characteristics in arbitrary superconducting structures was shown. The technique matches much slower 3D methods and is accurate for a wideband frequency range.

2.5.1 Closing remarks

The wideband frequency-response moves us closer to understanding the effect a long-distance PTL has on PTL-drivers and receivers. The next step is to convert the frequency-domain response into a time-domain simulation model.

Chapter 3

Superconductor time-domain modelling

3.1 Introduction

A macro-model is a simplified model that describes a much more complex system [29]. The macro-model can be used in place of the more complex model it describes while maintaining a high degree of accuracy without the unnecessary computational overhead [29]. With the frequency-dependent characteristics of PTL structures previously calculated, the next step is to find a simplified macro-model which can be used in time-domain simulations. In this chapter, the PTL structure will be explicitly handled, but the techniques used to model superconductivity are general and can be applied to any superconductor interconnect.

First, the per-unit-length parameter previously calculated has to be converted into a form that relates to voltage and current. The PTL is a frequency-dependent transmission line. The electrical response can be analytically described by solving the telegraph equations. The transmission line admittance, from [30], is given by

$$\mathbf{Y}_{TL} = \begin{bmatrix} \frac{1}{Z_L \tanh(\gamma l)} & \frac{-1}{Z_L \sinh(\gamma l)} \\ \frac{-1}{Z_L \sinh(\gamma l)} & \frac{1}{Z_L \tanh(\gamma l)} \end{bmatrix}, \tag{3.1}$$

where Z_L is the characteristics impedance of the line, γ is the propagation constant of the line, and l is the line length. Both Z_L, and γ are frequency dependent. The impedance, from [30], is given by

$$\mathbf{Z}_{TL} = \begin{bmatrix} \frac{Z_L}{\tanh(\gamma l)} & \frac{Z_L}{\sinh(\gamma l)} \\ \frac{Z_L}{\sinh(\gamma l)} & \frac{Z_L}{\tanh(\gamma l)} \end{bmatrix}. \tag{3.2}$$

The impedance and admittance of a fixed length PTL can be calculated from the previously calculated per-unit-length parameter together with equations (3.1) and (3.2). In this chapter, we will look at finding an accurate macro-model which fits the PTL's admittance and impedance for various line lengths.

3.2 Modelling

For superconductor interconnections, such as the PTL, it can be assumed that current signals are small, the temperature is constant, and non-linear proximity effects are negligible. From the assumptions, we can model superconductor interconnections as continuous linear time-invariant systems. The Josephson Junction is not linear and cannot be modelled using a linear system. However, modelling and simulation of the Josephson Junction is outside the scope of this thesis and is covered in other research [31; 32; 33]. We will, therefore, focus on the linear time-invariant case. This section discusses the theory behind linear time-invariant system modelling and how it pertains to modelling admittances and impedances.

3.2.1 Transfer Function

In a linear time-invariant system, we can define a system's impulse response as $h(t)$. Given an impulse response of a linear time-invariant system, $h(t)$, the output of the system is given by

$$y(t) = h(t) * u(t), \tag{3.3}$$

where $u(t)$ is a continuous input, and $y(t)$ is a continuous output. This relationship can be more conveniently expressed in the Laplace domain. Let $Y(s) = \mathcal{L}\{y(t)\}$, and $U(s) = \mathcal{L}\{u(t)\}$ then we can express $H(s)$ as

$$H(s) = \frac{Y(s)}{U(s)}. \tag{3.4}$$

The transfer function in (3.4) might not necessarily be in a form that is easily converted to the time domain. If $H(s)$ can be accurately approximated by a rational function,

$$H(s) \approx \frac{N(s)}{D(s)} = \frac{\sum_{i=0}^{n} a_i s^i}{\sum_{i=0}^{n} b_i s^i}, \tag{3.5}$$

then the transfer function can be efficiently converted to time-domain using recursive convolutions [34]. An excellent rational approximation can almost always be found for even complex electromagnetic responses. We will, therefore, use the rational approximation for our linear time-invariant models.

The impedance is a transfer function which takes the currents into the port as input and outputs the voltages at the ports. Similarly, the admittance is a transfer function which takes the voltages at the ports and outputs the current out of the ports. Transfer functions are, therefore, general enough to cover both impedances and admittances. For generality, we will work with transfer functions when possible.

3.2.2 Multi-port systems

The admittances and impedances for multiple ports take multiple inputs and produce multiple outputs. Admittances and impedances are, therefore, Multi-input Multi-output (MIMO) systems. The transfer function representation can be extended to a MIMO system by having a transfer function matrix, $\mathbf{H}(s)$, where each element corresponds to a single-input single-output system.

$$\mathbf{H}(s) = \begin{bmatrix} H_{11}(s) & \cdots & H_{1m}(s) \\ \vdots & \ddots & \vdots \\ H_{n1}(s) & \cdots & H_{nm}(s) \end{bmatrix}. \tag{3.6}$$

where $H_{ij}(s)$ is the output from the ith port as a result of the jth input. The input and output also then become vectors, $\mathbf{U}(s)$, and $\mathbf{Y}(s)$, respectively. The system is then defined as

$$\mathbf{Y}(s) = \mathbf{H}(s) \cdot \mathbf{U}(s). \tag{3.7}$$

3.2.3 State-Space Representation

Alternative to the transfer function representation, a system can be described by a state-space model. A state-space model defines a system in terms of the system's internal state, a vector $\mathbf{x}(t)$, the systems inputs, a vector $\mathbf{u}(t)$, and the systems outputs, a vector $\mathbf{y}(t)$. In the general case, it can be seen as a system where

$$\frac{d}{dt}\mathbf{x}(t) = \mathbf{f}(t, \mathbf{x}(t), \mathbf{u}(t)), \text{ and} \tag{3.8}$$

$$\mathbf{y}(t) = \mathbf{h}(t, \mathbf{x}(t), \mathbf{u}(t)). \tag{3.9}$$

This is an ordinary differential equation in time, and much research has gone into solving systems of the same form. In the linear time-invariant case where the system is not dependent on the derivative of the input the system can be simplified to a set of linear partial differential equations

$$\frac{d}{dt}\mathbf{x}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t), \text{ and} \tag{3.10}$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t), \tag{3.11}$$

where $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{D}$ are the state-space matrices that describe the system. In the Laplace domain, the equations become

$$s\mathbf{X}(s) = \mathbf{A}\mathbf{X}(s) + \mathbf{B}\mathbf{U}(s), \text{ and} \tag{3.12}$$

$$\mathbf{Y}(s) = \mathbf{C}\mathbf{X}(s) + \mathbf{D}\mathbf{U}(s). \tag{3.13}$$

The state-space representation of a transfer function is not unique, but a state-space representation maps to a specific transfer function. Equation (3.12) and (3.13)

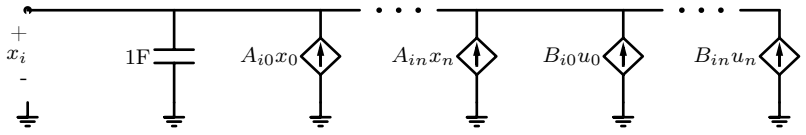

Figure 3.1: State-space variables as voltages

can be transformed by rearranging (3.12) and substituting the result into (3.13) to get

$$\mathbf{Y}(s) = \mathbf{C}\left(s\mathbf{I} - \mathbf{A}\right)^{-1}\mathbf{B}\mathbf{U}(s) + \mathbf{D}\mathbf{U}(s). \tag{3.14}$$

From (3.14) it is clear that the transfer function a state-space system represents is given by

$$\mathbf{H}(s) = \mathbf{C}\left(s\mathbf{I} - \mathbf{A}\right)^{-1}\mathbf{B} + \mathbf{D}. \tag{3.15}$$

Since many state-space representations exist for a single transfer function, there are multiple conversions from transfer function to state-space possible. The most convenient conversion depends on the form of the transfer function. The conversion will, therefore, be handled in the specific instances where required. For now, it is sufficient to know that a rational transfer function can be easily converted to a state-space model.

3.2.4 Equivalent SPICE model

If a state-state space representation of a system can be found, the system can be converted to an equivalent circuit [35; 36; 37]. The lumped model equivalent does not guarantee positive valued components [37]. For generality, we will adapt the more general and more abstract model, which uses dependent sources to model interactions [35; 36]. Instead of using equation defined dependent sources, we will use linear dependent sources as SPICE engines more widely support them.

State-space models contain as many unknowns as there are state variables. Each of these variables can be expressed as a current or as a voltage. If voltage nodes represent the state variables, then capacitance can be used to set up the derivative equation. Alternatively, if currents represent the state variables, then inductors can be used to set up the derivative equations.

Fig. 3.1 shows how the equations can be set up using capacitances and voltage nodes. Fig. 3.2 shows how the equations can be set up using inductors and currents. In both cases, the equations can be scaled for numerical stability.

SPICE engines use modified nodal analysis to solve the partial differential equation system [30; 38; 39]. When using modified nodal analysis, voltage sources require an additional unknown [30; 39], the current through the voltage source. All voltage nodes also correspond to an unknown in the system [30; 39]. For fast simulation, we will use voltages to represent the state variables as it will result in fewer unknowns.

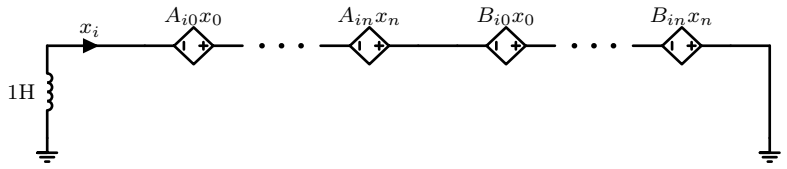

Figure 3.2: State-space variables as currents

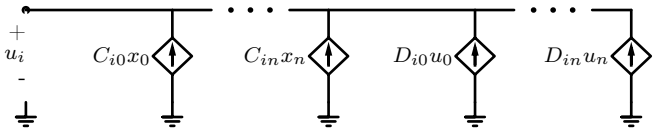

Figure 3.3: Admitance state-space implementation

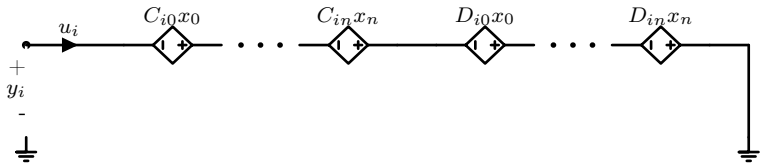

Figure 3.4: Impedance state-space implementation

Depending on what the state-space model represents, the input and output vectors can have different meanings. In the case of an admittance matrix, the input is the voltage over the ports, and the output is the current through the ports. In the case of an impedance matrix, the input is the current through the ports, and the output is the voltage over the ports.

Fig. 3.3 shows how an admittance state-space system is realized. Fig. 3.4 shows how an impedance state-space system is realized. The admittance state-space realization does not add any additional unknowns, where the impedance state-space realization generates intermediate voltage unknowns. The admittance representation should, therefore, be preferred if both representations are equally accurate.

3.3 Sanathanan-Koerner Iteration

To get an accurate SPICE model for a PTL, we need first to find an equivalent state-space system which represents the PTL. The problem can be rephrased as finding an accurate, rational approximation to the PTLs admittance or impedance transfer function. The problem, in general terms, is fitting a complex curve to sampled data

[40], with a rational function of the form

$$H(s) \approx H_{fit}(s) = \frac{N(s)}{D(s)} = \frac{\Phi_{N,0}(s) + \sum_{i=1}^{N_N} a_{N,i}\Phi_{N,i}(s)}{\Phi_{D,0}(s) + \sum_{i=1}^{N_D} a_{D,i}\Phi_{D,i}(s)}, \tag{3.16}$$

where N_N is number of numerator basis functions, N_D is the number of denominator basis functions, the unknowns, a_x, are real coefficients to predetermined basis functions, $\Phi_x(s)$. The basis functions, $\Phi_x(s)$, are required to be rational functions to ensure that $H_{fit}(s)$ is also a rational function.

Two main methodologies are used to solve the unknown coefficients in (3.16) [41]. Expectation-Maximization is a general statistical algorithm that can be applied to find a rational approximation to a complex curve [41]. Vector-Fitting is an iterative least-squares algorithm that was developed specifically for finding a rational approximation to a given frequency response [42]. Vector-Fitting tends to yield better fits and can be easily adapted to ensure the stability and accuracy of the model in numerous circumstances [41]. Accordingly, this thesis will focus on Vector-Fitting and how it needs to be adapted for superconductor models.

The Vector-Fitting algorithm [42] will be explained in terms of Sanathanan-Kroener iteration [43; 44] as the explanation is, subjectively, more straightforward than the original explanation.

3.3.1 Pole relocation

The error of the rational approximation is the difference between the actual frequency response and that of the rational approximation. This can be put mathematically as

$$E(s) = H(s) - H_{fit}(s) \tag{3.17}$$

$$= H(s) - \frac{N(s)}{D(s)}. \tag{3.18}$$

The error, $E(s)$, in equation (3.18) can be minimized using non-linear least-squares optimization techniques. Unfortunately, the strong non-linearity caused by the denominator polynomial makes the optimization unstable.

The non-linearity can be removed by multiplying (3.18) with $D(s)$, leading to

$$E(s)D(s) = H(s)D(s) - N(s). \tag{3.19}$$

The term, $E(s)D(s)$, in equation (3.19), can be minimized using linear least-squares optimization, but the denominator will weight the error. Therefore, the fitted approximation will be less accurate close to the poles of the approximation.

The problem can be mitigated by iteratively weighting the minimization by the previously calculated poles. The function being minimized then becomes

$$E'(s) = \frac{E(s)D_n(s)}{D_{n-1}(s)} = \frac{H(s)D_n(s)}{D_{n-1}(s)} - \frac{N_n(s)}{D_{n-1}(s)}. \tag{3.20}$$

This iteration scheme, shown in equation (3.20), is known as Sanathanan-Koerner iteration. Given discrete samples at different frequency points, $(s_1, s_2, \ldots, s_k)$, the minimization of (3.20) corresponds to the solution of the overdetermined set of equations

$$0 \approx \frac{H(s_i)D_n(s_i)}{D_{n-1}(s_i)} - \frac{N_n(s_i)}{D_{n-1}(s_i)} \;\forall\; i = 1, 2, \ldots, k. \tag{3.21}$$

The denominator determines the poles of the system. The poles of the system are, therefore, iteratively relocated until the iteration scheme finished.

In practice, not all frequencies are equally important. Depending on the usage of the fitted approximation, different frequency samples might be more important and should be weighted more. A weighting term is added to (3.21) which results in

$$0 \approx \frac{w(s_i)H(s_i)D_n(s_i)}{D_{n-1}(s_i)} - \frac{w(s_i)N_n(s_i)}{D_{n-1}(s_i)} \;\forall\; i = 1, 2, \ldots, k. \tag{3.22}$$

3.3.2 Final Fitting

The numerator coefficients are also solved in (3.21), but after every iteration a newer and better set of poles are available. After the poles have been fixed, the numerator should be updated again with the final poles. After iteration n, the minimization of (3.18) corresponds to the solution of the overdetermined set of equations

$$H(s_i) \approx \frac{N(s_i)}{D_n(s_i)} \;\; \forall\; i = 1, 2, \ldots, k. \tag{3.23}$$

Equation (3.23) is linear as the denominator is fixed. Simlarly to the weighting in (3.22) we have to weight (3.23) which results in

$$w(s_i)H(s_i) \approx \frac{w(s_i)N(s_i)}{D_n(s_i)} \;\; \forall\; i = 1, 2, \ldots, k. \tag{3.24}$$

3.3.3 Basis function

Up until now, we have not specified anything of the basis functions other than that they are rational functions. The choice of basis functions in Sanathanan-Koerner iteration is critical, but the exact requirements of the basis functions are not appropriately handled in literature.

The basis function for every iteration does not have to be the same. It is also recommended that the basis function is updated every iteration for numerical stability.

The numerator and denominator function space is defined as

$$\Phi_X(s) = \frac{w_X(s)X_n(s)}{D_{n-1}(s)} = \Phi_{X,0}(s) + \sum_{i=1}^{N_X} a_{X,i}\Phi_{X,i}(s), \tag{3.25}$$

where $w_X(s)$ is an additional weighting. The additonal weighting exist so that the numerator and denominator function space can absorb the weighting term, $w(s)$, or the transfer function term, $H(s)$.

The function space as defined by (3.25) are more general than what we need. To allow our implementation to be general and use the same function space for both numerator and denominator we always have $w_X(s) = 1$. We do not require the basis functions to be affine for fitting superconductor admittances and impedances. Our function spaces can be linear with $\Phi_{X,0(s)} = 0$. Our function space then becomes

$$\Phi_X(s) = \frac{X_n(s)}{D_{n-1}(s)} = \sum_{i=1}^{N_X} a_{X,i}\Phi_{X,i}(s). \tag{3.26}$$

The denominator function space also has to be proper, but not strictly proper. Alternatively put, the denominator function space should have the same amount of zeros and poles. If denominator function space does not have the same amount of zeros and poles, the degree of the fitting will change between iterations.

We will dedicate a section to the numerical implementation and the different basis functions we use.

3.3.4 Uniqueness constraint

One might have noticed that for any solution $\frac{N(s)}{D(s)}$ we have infinite equivalent solutions of the form $\frac{\alpha N(s)}{\alpha D(s)}$, where $\alpha \in \mathbb{R}$. To remove this ambiguity in the formulation, we have to add a constraint which guarantees a unique solution. The constraint can be added by using an affine function space instead of a linear function space. This is done in the original vector fitting article where $\Phi_{D,0}(s)$ was defined as one [42].

We will not follow this approach as we find it beneficial to let an additional equation define the uniqueness constraint. Using a uniqueness constraint equation allows the uniqueness constraint to be changed without changing our formulation or implementation. It was also later shown that having a relaxed uniqueness constraint has advantages when fitting systems with noise [45].

As the uniqueness constraint will only be enforced in the least-squares sense, it is crucial to have the constraint weighted enough so that its error is not considered negligible and not too much to cause ill-conditioning of the overall system. Following the recommendation of [45] we scale the uniqueness constraint equation so that its error is proportional to the average of the weighted sampled transfer functions.

Two uniqueness constraints appear in publications [42; 45]. The most widely used uniqueness constraint is the one used in the original vector fitting article. In the original article [42], the uniqueness constraint enforced

$$\lim_{s\to\infty} \Phi_D(s) = 1. \tag{3.27}$$

This is equivalent to forcing the denominator function to be unity at high frequencies [42]. The other published constraint is known as the relaxed constraint [45], it

enforces

$$\Re\left\{\sum_{j=1}^{N_s}\left(\sum_{i=1}^{N_D}\Phi_i(s_j)\right)\right\} = N_s. \tag{3.28}$$

This is equivalent as enforcing the sum of the real part of $\frac{D_n(s)}{D_{n-1}(s)}$ to be non-zero. Upon converging, $\frac{D_n(s)}{D_{n-1}(s)}$ will be unity.

The relaxed uniqueness constraint has benefits when the simulation is noisy, but our transfer functions are exact. We will, therefore, use the original constraint as specified in the original vector fitting article.

The equation from the uniqueness constraint all have the following form

$$w_c \sum_{i=0}^{N_D} a_{C,i} a_{D,i} \approx w_c, \tag{3.29}$$

where w_c is the uniqueness constraint weighting, and $a_{C,i}$ is the constraint coefficients.

3.3.5 System of equations

The overconstrained system of equations, (3.22), can be solved using linear least squares minimization. Following the sign convention most commonly used in literature we negate equation (3.22). The system of equations then become

$$0 \approx w(s_i)\sum_{j=1}^{n} a_{D,j}\Phi_{D,j}(s_i) - w(s_i)H(s_i)\sum_{j=1}^{N_D} a_{D,j}\Phi_{D,j}(s_i)\ \forall\ i = 1, 2, \ldots, k. \tag{3.30}$$

Equation system, (3.30) along with uniqueness constraint, (3.29), can be written in matrix form

$$\begin{bmatrix} \mathbf{W}_d \cdot \Phi_N & -\mathbf{H}_d \cdot \mathbf{W}_d \cdot \Phi_D \\ \mathbf{0} & w_C \mathbf{a}_C^T \end{bmatrix} \cdot \begin{bmatrix} \mathbf{a_N} \\ \mathbf{a_D} \end{bmatrix} \approx \begin{bmatrix} \mathbf{0} \\ w_c \end{bmatrix} \tag{3.31}$$

where

$$\mathbf{\Phi}_X = \begin{bmatrix} \Phi_{X,1}(s_1) & \cdots & \Phi_{X,n}(s_1) \\ \vdots & \ddots & \vdots \\ \Phi_{X,1}(s_k) & \cdots & \Phi_{X,n}(s_k) \end{bmatrix}, \tag{3.32}$$

$$\mathbf{H}_d = \begin{bmatrix} H(s_1) & 0 & \cdots & 0 \\ 0 & H(s_2) & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & H(s_k) \end{bmatrix}, \text{ and} \tag{3.33}$$

$$\mathbf{W}_d = \begin{bmatrix} w(s_1) & 0 & \cdots & 0 \\ 0 & w(s_2) & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & w(s_k) \end{bmatrix}. \tag{3.34}$$

Equation (3.22) is complex, but require real coefficients. The real and imaginary part is separated to get a purely real system of equations,

$$\begin{bmatrix} \Re\{\mathbf{W}_d \cdot \Phi_N\} & -\Re\{\mathbf{H}_d \cdot \mathbf{W}_d \cdot \Phi_D\} \\ \Im\{\mathbf{W}_d \cdot \Phi_N\} & -\Im\{\mathbf{H}_d \cdot \mathbf{W}_d \cdot \Phi_D\} \\ \mathbf{0} & w_C \mathbf{a}_C^T \end{bmatrix} \cdot \begin{bmatrix} \mathbf{a_N} \\ \mathbf{a_D} \end{bmatrix} \approx \begin{bmatrix} \mathbf{0} \\ \mathbf{0} \\ w_C \end{bmatrix} \tag{3.35}$$

The overconstrained system of equation in (3.35) can be solved using linear least squares.

3.3.6 Numerical considerations

Sanathanan-Koerner iteration can potentially be numerically unstable [46]. Without careful considerations when implementing (3.35) one might get large numerical error [46]. The numerical error comes from the condition number of the system matrix in (3.35) [46]. The numerical error can be large enough to prevent the iteration process from converging and can also produce unusably poor fittings.

It is mentioned a few times in literature that normalizing the matrix columns results in improved conditioning [46; 47; 48]. We have found that not normalizing the columns makes the procedure fragile. The unnormalized system performed well when a rational function exactly represents the transfer function. Unfortunately, in problems where it is a difficult fit, such as is the case with a PTL, the results were mostly unusable when a higher-order fit was attempted. We, therefore, recommend that the columns are always normalized.

The other large contributor to the condition number of the system matrix is the choice of basis function [44; 46]. The conditioning of the linear least squares problem, $\mathbf{Ax} \approx \mathbf{b}$, depends on the conditioning of $\mathbf{AA}^T$. The conditioning of the system matrix, therefore, depends on the conditioning of $\mathbf{\Phi}_X \mathbf{\Phi}_X^T$. The basis function is discussed in detail in the next section.

3.4 Basis Functions

The mathematical definition of the basis function is given in 3.3.3. This is enough to formulate the problem, but is not sufficient to define what is required from an implementation.

From a mathematical viewpoint, it is required that Sanathanan-Koerner function spaces have basis functions of the form $\frac{X(s)}{D_{n-1}(s)}$. It is further required that the denominator function space should have the same amount of zeros as poles. Implicitly, the zeros of the denominator function space should be calculatable.

From an implementation viewpoint, we will also require that the state-space matrices should be constructible from the function space coefficients. This might seem unnecessary, but in practice, the zeros of rational transfer functions are calculated by converting the transfer function into state-space representation and solving the zeros of the state-space system. Being able to construct the state-space system from the final fit is also essential for using the model in further simulations.

Zeros of state-space system

As previously stated the zeros of the transfer function has to be calculated. In our implementation, we will always calculate the zeros of the transfer function by calculating the zeros of the state-space system.

Given that $\mathbf{Y}(s) = 0$, we can rewrite (3.12), and (3.13) to

$$\left(\mathbf{A} - \mathbf{B}\mathbf{D}^{-1}\mathbf{C}\right)\mathbf{X}(s) = s\mathbf{X}(s). \tag{3.36}$$

From (3.36), we can see that the zeros correspond to the eigenvalues of $\left(\mathbf{A} - \mathbf{B}\mathbf{D}^{-1}\mathbf{C}\right)$. However, $\mathbf{D}$ is not always invertible, and (3.36) is only usable if $\mathbf{D}$ is invertible.

Fortunately, we only have to be able to find the zeros of the denominator function space, and for the denominator function space to have as many zeros as poles, D is required to be invertible. In the case where a relaxed constraint is used, the solution can be almost zero [45]. This makes the calculation of the zeros of the state-space system of the denominator function space numerically unstable. If this happens, then different uniqueness constraint should be used [45]. We do not use a relaxed uniqueness constraint, so we do not have to follow this procedure, but due to our general implementation and formulation, this is trivial to implement.

3.4.1 Polynomial basis functions

The naive choice of basis function is a monomial series of increasing order weighted by the denominator. In the original article on Sanathanan-Koerner iteration, the authors used this basis [43]. The monomial basis function is defined as

$$\Phi_i(s) = \frac{s^i}{D_{n-1}(s)}. \tag{3.37}$$

However, one can factorize a Vandermonde from $\mathbf{\Phi}\mathbf{\Phi}^T$ [46]. Vandermonde matrices rapidly become ill-conditioned for higher powers [49]. This ill-conditioning severely limits the order of the rational function that can be fitted.

Due to the limitations of the monomial series basis functions, it cannot be used to fit the admittance and impedance characteristic of a passive transmission line. Accordingly, we will not spend any further time expanding on the polynomial basis function.

3.4.2 Rational basis functions

The usage of rational basis functions comes from the original Vector Fitting article [42]. In the original Vector Fitting article the iteration scheme used a new formulation but was later shown to be a generalization of Sanathanan-Koerner iteration with rational basis functions [44]. The use of rational basis function made the iteration scheme stable enough for most higher-order fittings [42; 46].

The partial fraction expansion of (3.5), leads to

$$H(s) \approx \sum_{i=1}^{N_P} \frac{r_i}{s - p_i} + \sum_{i=0}^{N_R} d_i s_i, \tag{3.38}$$

where N_P is the number of poles in the system, and N_R is the remaining order after $N(s)$ and $D(s)$ van be factorized. From (3.38), it follows that one can use each partial fraction as a basis [42]. If the remainder is omitted, the basis function is then defined as

$$\Phi_i(s) = \frac{1}{s - p_i}. \tag{3.39}$$

The state-space realization of the rational basis function can be obtained by connecting the state-space realization of the individual poles in parallel [42; 46].

$$\mathbf{A} = \begin{bmatrix} p_1 & 0 & \cdots & 0 \\ 0 & p_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & p_n \end{bmatrix}, \tag{3.40}$$

$$\mathbf{B} = \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix}, \tag{3.41}$$

$$\mathbf{C} = \begin{bmatrix} r_1 \\ \vdots \\ r_n \end{bmatrix}^T, \text{ and} \tag{3.42}$$

$$\mathbf{D} = \begin{bmatrix} d \end{bmatrix}. \tag{3.43}$$

Since complex poles and residues come in pairs, a slight modification has to be made [42]. The basis functions for the corresponding complex pole pair can be transformed so that real coefficients, a_i and a_{i+1}, correspond to the real and imaginary part of the complex residue pair [42]. Given that the complex pole pairs are placed such that $p_i = p_{i+1}^*$ then

$$\Phi_i(s) = \frac{1}{s - p_i} + \frac{1}{s - p_i^*}, \text{ and} \tag{3.44}$$

$$\Phi_{i+1}(s) = \frac{j}{s - p_i} - \frac{j}{s - p_i^*} \tag{3.45}$$

The submatrices which correspond to the complex pole pairs have to, consequently, be transformed [42]. The submatrices become

$$\mathbf{A} = \begin{bmatrix} \Re(p) & \Im(p) \\ -\Im(p) & \Re(p) \end{bmatrix}, \tag{3.46}$$

$$\mathbf{B} = \begin{bmatrix} 2 \\ 0 \end{bmatrix}, \text{ and} \tag{3.47}$$

$$\mathbf{C} = \begin{bmatrix} \Re(r) \\ \Im(r) \end{bmatrix}^T. \tag{3.48}$$

The basis function matrix, $\mathbf{\Phi}$, which closely resembles a Cauchy-matrix [46], is significantly better conditioned than the monomial basis function. This improved conditioning is what makes it possible to do higher-order fitting. The problem becomes ill-conditioned if the real part of the complex pole pairs becomes too large relative to their imaginary component [46]. According to [46], most physical systems have poles with relatively small real components.

3.4.3 Orthonormal

For optimal conditioning, the basis functions should be orthonormal [46]. This entails that

$$\langle \Phi_i, \Phi_j \rangle = \begin{cases} 1, & \text{if } i = j \\ 0, & \text{otherwise} \end{cases}. \tag{3.49}$$

The problem is discrete so the inner product is defined as

$$\langle \Phi_i, \Phi_j \rangle = \frac{1}{2j\pi k} \sum_{n=0}^{k} \Phi_i(s_n) \Phi_j(s_n)^*. \tag{3.50}$$

This requires a numerical orthonormalization procedure, such as the Gram-Schmidt procedure, to attain the basis functions [46]. If the frequency samples are evenly and finely spaced, and no poles sit very close to the edges of the sampled response, then the basis function can be accurately approximated as a continuous integral

$$\langle \Phi_i, \Phi_j \rangle = \frac{1}{2j\pi} \int_{j\mathbb{R}} \Phi_i(s) \Phi_j(s)^* ds. \tag{3.51}$$

To not delve into unnecesary detail we will only present the basis function and their state-space representation, as in [46], here. For a detailed account see the Orthonormal Vector Fitting publication [46]. Orthonormal rational basis functions are defined as

$$\Phi_i(s) = \sqrt{-2\Re\{p_i\}} \left(\prod_{j=1}^{i-1} \frac{s + p_i^*}{s - p_i} \right) \frac{1}{s - p_i} \tag{3.52}$$

which is realized with the following state-space system

$$\mathbf{A} = \begin{bmatrix} p_1 & 0 & \cdots & 0 \\ \Re\{p_1\} & p_2 & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ \Re\{p_1\} & \cdots & \Re\{p_{n-1}\} & p_n \end{bmatrix}, \tag{3.53}$$

$$\mathbf{B} = \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix}, \tag{3.54}$$

$$\mathbf{C} = \begin{bmatrix} a_1\sqrt{-2\Re\{p_1\}} \\ \vdots \\ a_n\sqrt{-2\Re\{p_n\}} \end{bmatrix}^T, \text{ and} \tag{3.55}$$

$$\mathbf{D} = \begin{bmatrix} d \end{bmatrix}. \tag{3.56}$$

Similarly to the rational basis function case, the basis function has to be transformed to guarantee complex pole pairs. The transformed basis functions are

$$\Phi_i(s) = \sqrt{-2\Re\{p_i\}} \left(\prod_{j=1}^{i-1} \frac{s+p_i^*}{s-p_i} \right) \frac{s-|p_i|}{(s-p_i)(s-p_i^*)}, \text{ and} \tag{3.57}$$

$$\Phi_{i+1}(s) = \sqrt{-2\Re\{p_i\}} \left(\prod_{j=1}^{i-1} \frac{s+p_i^*}{s-p_i} \right) \frac{s+|p_i|}{(s-p_i)(s-p_i^*)}. \tag{3.58}$$

The A state-space submatrix then has to be replaced by

$$\mathbf{A} = \begin{bmatrix} \Re(p) & \Re(p)-|p_i| \\ \Re(p)+|p_i| & \Re(p) \end{bmatrix}. \tag{3.59}$$

while the rest of the matrices remain unchanged.

The orthonormal rational basis functions remain well conditioned even if the starting poles are chosen poorly, or the transfer function has poles with large real components. We recommend always using orthonormal rational basis functions during the pole-relocation process.

3.4.4 Closing remarks

One might be tempted only to use orthonormal basis functions as they provide excellent conditioning. Unfortunately, they have dense state-space matrices. Rational basis functions provide sparse state-space matrices but can have poor conditioning in certain circumstances [46]. However, rational basis functions do have good conditioning when the poles are close to optimal [46].

A good strategy would be to use orthonormal basis functions during the pole relocation process and switch over to rational basis function during the final fitting process. This ensures that the pole relocation process is numerically stable and that the final fitted state-space matrices are sparse. This is why it is so important to have a formulation and implementation which is agnostic to the basis function being used.

3.5 Vector Fitting

So far, the fitting of a single-port system has been discussed. A single port system is very seldom sufficient to describe practical systems. Even a simple resistive connection has two ports. It is, therefore, necessary to extend the system identification to MIMO systems.

The name, Vector Fitting, comes from fitting vector-valued functions. The extension of the vector fitting formulation to handle vector-valued function also applies to Sanathanan-Koerner iteration. We will continue with the Sanathanan-Koerner iteration formulation.

3.5.1 Multi-port systems

A MIMO system can be seen as the sum of separate SISO systems [50]. The simplest way to fit a multi-port system is then to fit the individual transfer function matrix entries and construct the MIMO system from the individual SISO systems.

Lets denote the fit of transfer function matrix entry, $H_{ij}(s)$, as $H_{ij}^{fit}(s)$. $H_{ij}(s)$ has the following state space matrices $A_{ij}, B_{ij}, C_{ij}, D_{ij}$. The transfer funciton matrix, H^{fit}, then has the following state space matrices:

$$\mathbf{A} = \begin{bmatrix} \mathbf{A}_{11} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{A}_{12} & \ddots & \vdots \\ \vdots & \ddots & \ddots & \mathbf{0} \\ \mathbf{0} & \cdots & \mathbf{0} & \mathbf{A}_{nm} \end{bmatrix}, \tag{3.60}$$

$$\mathbf{B} = \begin{bmatrix} \mathbf{B}_{11} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{B}_{12} & \ddots & \vdots \\ \vdots & \ddots & \ddots & \mathbf{0} \\ \vdots & & \ddots & \mathbf{B}_{1m} \\ \vdots & & & \mathbf{0} \\ \mathbf{0} & & & \vdots \\ \mathbf{B}_{n1} & \ddots & & \vdots \\ \mathbf{0} & \mathbf{B}_{n2} & \ddots & \vdots \\ \vdots & \ddots & \ddots & \mathbf{0} \\ \mathbf{0} & \cdots & \mathbf{0} & \mathbf{B}_{nm} \end{bmatrix}, \tag{3.61}$$

$$\mathbf{C} = \begin{bmatrix} \mathbf{C}_{11} & \mathbf{0} & \cdots & \cdots & \mathbf{0} \\ \vdots & \vdots & & & \vdots \\ \mathbf{C}_{1m} & \mathbf{0} & & & \vdots \\ \mathbf{0} & \mathbf{C}_{21} & \mathbf{0} & & \vdots \\ \vdots & \vdots & \vdots & & \vdots \\ \mathbf{0} & \mathbf{C}_{2m} & \mathbf{0} & & \vdots \\ \vdots & \ddots & \ddots & \ddots & \vdots \\ \vdots & & \ddots & \ddots & \mathbf{0} \\ \vdots & & & \mathbf{0} & \mathbf{C}_{n1} \\ \vdots & & & \vdots & \vdots \\ \mathbf{0} & \cdots & \cdots & \mathbf{0} & \mathbf{C}_{nm} \end{bmatrix}^T, \text{ and} \tag{3.62}$$

$$\mathbf{D} = \begin{bmatrix} D_{11} & \cdots & D_{1m} \\ \vdots & \ddots & \vdots \\ D_{n1} & \cdots & D_{nm} \end{bmatrix}. \tag{3.63}$$

The resulting MIMO state-space system quickly becomes large for a large number of ports. A better method for a MIMO system is required.

3.5.2 Common pole optimization

If each of the SIMO systems in the MIMO system has a common pole structure, the state-space representation can be greatly simplified. The **A**, **B**, and **C** state-space matrices then become

$$\begin{bmatrix} \mathbf{A}_1 & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{A}_2 & \ddots & \vdots \\ \vdots & \ddots & \ddots & \mathbf{0} \\ \mathbf{0} & \cdots & \mathbf{0} & \mathbf{A}_n \end{bmatrix}, \tag{3.64}$$

$$\mathbf{B} = \begin{bmatrix} \mathbf{B}_1 & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{B}_2 & \ddots & \vdots \\ \vdots & \ddots & \ddots & \mathbf{0} \\ \mathbf{0} & \cdots & \mathbf{0} & \mathbf{B}_n \end{bmatrix}, \text{ and} \tag{3.65}$$

$$\mathbf{C} = \begin{bmatrix} \mathbf{C}_{11} & \cdots & \mathbf{C}_{1m} \\ \vdots & \ddots & \vdots \\ \mathbf{C}_{n1} & \cdots & \mathbf{C}_{nm} \end{bmatrix}. \tag{3.66}$$

Fitting multiple transfer functions with a common pole set would substantially reduce the resulting state-space model. Hence, the need for vector fitting.

3.5.3 System of equations

In the vector fitting process, each numerator has its own set of coefficients, but all share the same pole coefficients. The system of equations corresponding to each individual transfer function is shown in (3.67).

$$\begin{bmatrix} \Re\{\mathbf{W}_i\mathbf{\Phi}_i\} & -\Re\{\mathbf{W}_i\mathbf{H}_i\mathbf{\Phi}\} \\ \Im\{\mathbf{W}_i\mathbf{\Phi}_i\} & -\Im\{\mathbf{W}_i\mathbf{H}_i\mathbf{\Phi}\} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{a}_i \\ \tilde{\mathbf{a}} \end{bmatrix} \approx \begin{bmatrix} \mathbf{0} \\ \mathbf{0} \end{bmatrix}, \tag{3.67}$$

Combining all the system of equations of the individual transfer functions, (3.67), with the uniqueness constraints results in (3.68).

$$\begin{bmatrix} \Re\{\mathbf{W}_1\mathbf{\Phi}_1\} & \mathbf{0} & \cdots & \cdots & \mathbf{0} & -\Re\{\mathbf{W}_1\mathbf{H}_1\mathbf{\Phi}\} \\ \Im\{\mathbf{W}_1\mathbf{\Phi}_1\} & \mathbf{0} & & & \mathbf{0} & -\Im\{\mathbf{W}_1\mathbf{H}_1\mathbf{\Phi}\} \\ \mathbf{0} & \Re\{\mathbf{W}_2\mathbf{\Phi}_2\} & \mathbf{0} & & \vdots & -\Re\{\mathbf{W}_2\mathbf{H}_2\mathbf{\Phi}\} \\ \mathbf{0} & \Im\{\mathbf{W}_2\mathbf{\Phi}_2\} & \mathbf{0} & & \vdots & -\Im\{\mathbf{W}_2\mathbf{H}_2\mathbf{\Phi}\} \\ \vdots & \ddots & \ddots & \ddots & \vdots & \vdots \\ \vdots & & \ddots & \ddots & \mathbf{0} & \vdots \\ \vdots & & & \mathbf{0} & \Re\{\mathbf{W}_n\mathbf{\Phi}_n\} & -\Re\{\mathbf{W}_n\mathbf{H}_n\mathbf{\Phi}\} \\ \vdots & & & \vdots & \Im\{\mathbf{W}_n\mathbf{\Phi}_n\} & -\Im\{\mathbf{W}_n\mathbf{H}_n\mathbf{\Phi}\} \\ \mathbf{0} & \cdots & \cdots & \mathbf{0} & \mathbf{0} & \mathbf{c}_T \end{bmatrix} \cdot \begin{bmatrix} \mathbf{a}_1 \\ \mathbf{a}_2 \\ \vdots \\ \mathbf{a}_n \\ \tilde{\mathbf{a}} \end{bmatrix} \approx \begin{bmatrix} \mathbf{0} \\ \vdots \\ \vdots \\ \mathbf{0} \\ \mathbf{1} \end{bmatrix} \tag{3.68}$$

3.5.4 Fast implementation

The system matrix in (3.68) is sparse, and a substantial speed-up can be obtained by using a sparse solver [51]. The solution of the numerator coefficients during the pole relocation process is also unused [51]. The numerator coefficients are uncoupled from each other [51]. This sparsity pattern can be exploited [51]. Following [51], we apply QR-factorization to (3.69), and by multiplying both sides with the transpose of the unitary matrix, Q_i, we arrive at (3.70).

$$\begin{bmatrix} \mathbf{Q}_i \end{bmatrix} \cdot \begin{bmatrix} \mathbf{R}_{i,11} & \mathbf{R}_{i,12} \\ \mathbf{0} & \mathbf{R}_{i,22} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{a}_i \\ \tilde{\mathbf{a}} \end{bmatrix} \approx \begin{bmatrix} \mathbf{0} \\ \mathbf{0} \end{bmatrix} \tag{3.69}$$

$$\begin{bmatrix} \mathbf{R}_{i,11} & \mathbf{R}_{i,12} \\ \mathbf{0} & \mathbf{R}_{i,22} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{a}_i \\ \tilde{\mathbf{a}} \end{bmatrix} \approx \begin{bmatrix} \mathbf{Q}_i^T \end{bmatrix} \cdot \begin{bmatrix} \mathbf{0} \\ \mathbf{0} \end{bmatrix} \tag{3.70}$$

The denominator coefficients of the new system of equations, (3.70), are not dependent on the numerator coefficeints [51]. Only the denominator part, (3.71), of (3.70) has to be solved [51].

$$\begin{bmatrix} \mathbf{R}_{i,22} \end{bmatrix} \cdot \begin{bmatrix} \tilde{\mathbf{a}} \end{bmatrix} \approx \begin{bmatrix} \mathbf{0} \end{bmatrix} \tag{3.71}$$

Combining all equations from all the transfer functions along with the uniqueness constraint gives us (3.72).

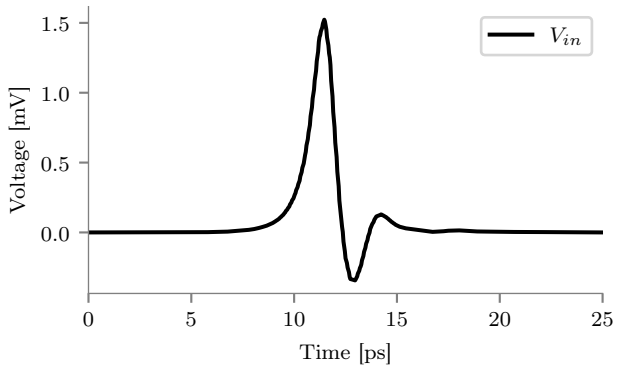

Figure 3.5: SFQ Pulse used as a test waveform

$$\begin{bmatrix} \mathbf{R}_{1,22} \\ \mathbf{R}_{2,22} \\ \vdots \\ \mathbf{R}_{n,22} \\ \mathbf{c}_T \end{bmatrix} \cdot \left[\tilde{\mathbf{a}}\right] \approx \begin{bmatrix} \mathbf{0} \\ \vdots \\ \vdots \\ \mathbf{0} \\ \mathbf{1} \end{bmatrix} \tag{3.72}$$

Solving (3.72) gives a substantial computation speed-up compared to the original system of equations, (3.68). This formulation is known as the fast vector fitting formulation [51].

3.6 Superconductor Vector Fitting

Before a moderately sized PTL structure is investigated we first look at a short 10 µm long line. An inductor segment well represents the short line's admittance. We can, therefore, use this short line as a test to see that our model operates as expected. For a test signal, we extracted an SFQ waveform from the output train of a DC-SFQ converter. The test signal is shown in Fig. 3.5, and the inductive response is shown in Fig. 3.6. I_1 refers to the current into the first port and I_2 refers to the current out of port 2.

Using (3.1) and the per-unit parameters calculated from our example PTL in section 2.4 we calculate addmitance of the 10 µm long PTL. The addmitance is fitted using the previously described vector fitting algorithm. An excellent fit is achieved by using six complex pole pairs.

Due to the size of the fitted model, we will not include the model details. The model is a rational approximation, and the poles and residues have no physical meaning, and, therefore, no reasonable subset of the model can be shown in isolation either. All information that the model provides can be seen in the frequency response of the model. Hence, we will only show the frequency response of all fitted models.

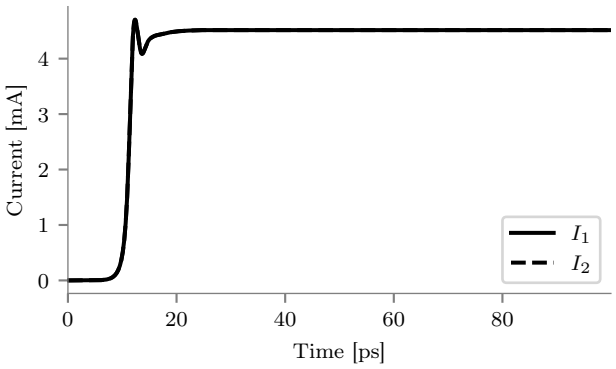

Figure 3.6: Inductive response to the test waveform

The reference and fitted admittance of the 10 µm long PTL is shown in Fig. 3.7, and Fig. 3.8 respectively.

The extracted state-space system is converted to JoSIM SPICE format and run with the same test waveform as the inductor approximation. The resulting current plot is shown in Fig. 3.9.

The resulting waveform is initially correct, but starts dissapating current continuously. Not shown in the plot, but the current dissapates to zero given enough time. The fitted model does not trap flux as expected. This approximation is passable if the model is never used in a situation where it might trap flux and is unsensitive to the very low frequency characteristics of the model. This unexpected behaviour might cause some suprises when used in a larger more complicated design simulations. How would one verify that flux is not accidentally trapped in the PTL if the approximated model prevents it? It is therefore required to identify what is happening during the fitting process and how to correctly fit a superconductor model.

3.6.1 Superconductor requirements

Superconductors have ideal DC responses due to their unique properties. First, the responses must be characterized in terms of admittance, impedance, and scattering parameters. Given an n port system where port i that is connected to ground with a superconductor then

$$\lim_{\omega\to 0} Y_{ii}(\omega) = \lim_{\omega\to 0} \frac{1}{j\omega L_{ii}} = -j\infty, \tag{3.73}$$

$$\lim_{\omega\to 0} Z_{ii}(\omega) = \lim_{\omega\to 0} j\omega L_{ii} = 0, \text{ and} \tag{3.74}$$

$$\lim_{\omega\to 0} S_{ij}(\omega) = \begin{cases} -1, & \text{if } i = j \\ 0, & \text{otherwise} \end{cases} \forall\ j = 1, \ldots, n. \tag{3.75}$$

where L_{ii} is the equivalent inductance to ground of the ith port. The ports of the admittance are considered shorted, and (3.73) is also true if it is connected with

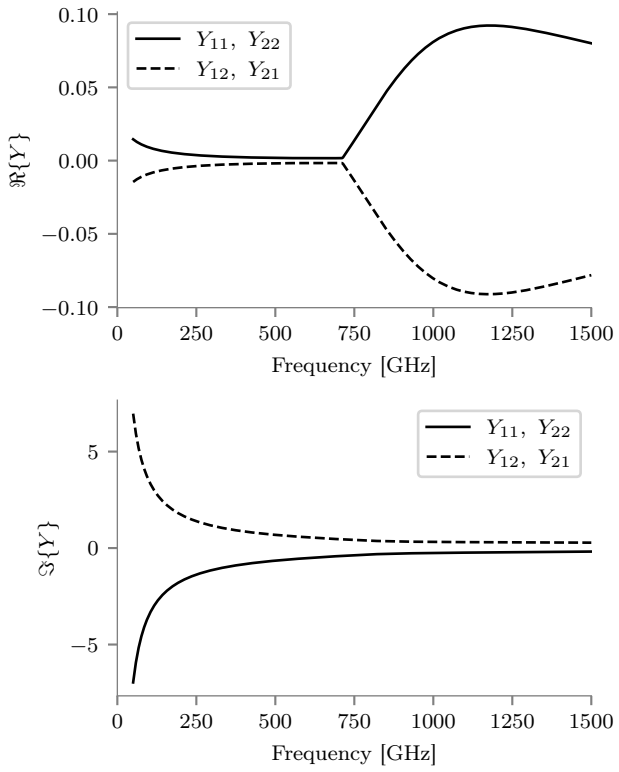

Figure 3.7: Admittance of the 10 µm long PTL

a superconductor to another port.

Given an n-port system where port i is connected with a superconductor to ports j_x then

$$\lim_{\omega\to 0} Y_{ij}(\omega) = \lim_{\omega\to 0} \frac{-1}{j\omega L_{ij}} = j\infty, \tag{3.76}$$

$$\lim_{\omega\to 0} Z_{ij}(\omega) = \lim_{\omega\to 0} j\omega L_{ij} = 0, \text{ and} \tag{3.77}$$

$$1 = -\lim_{\omega\to 0} S_{ii}(w) + \lim_{\omega\to 0} \sum_{x} S_{ij_x}(w). \tag{3.78}$$

In the admittance case of our PTL, we, therefore, have a pole at $\omega = 0$, which is outside the fitting range. The pole can, also, never be within the fitting range as it would require a numerical infinity at $\omega = 0$. The inaccuracies of fitting a function with a pole outside the fitting range are already mentioned in [42]. We observe precisely the error that is observed in [42]. The fit is accurate in the fitting range with large errors outside of the fitting range around the external pole.

It would be tempting to just fit the impedance with $w = 0$ included in the fitting range, but the system of equations is enforced in a least-squares sense. The impedance would not be exactly 0, which is the requirement for the model to behave

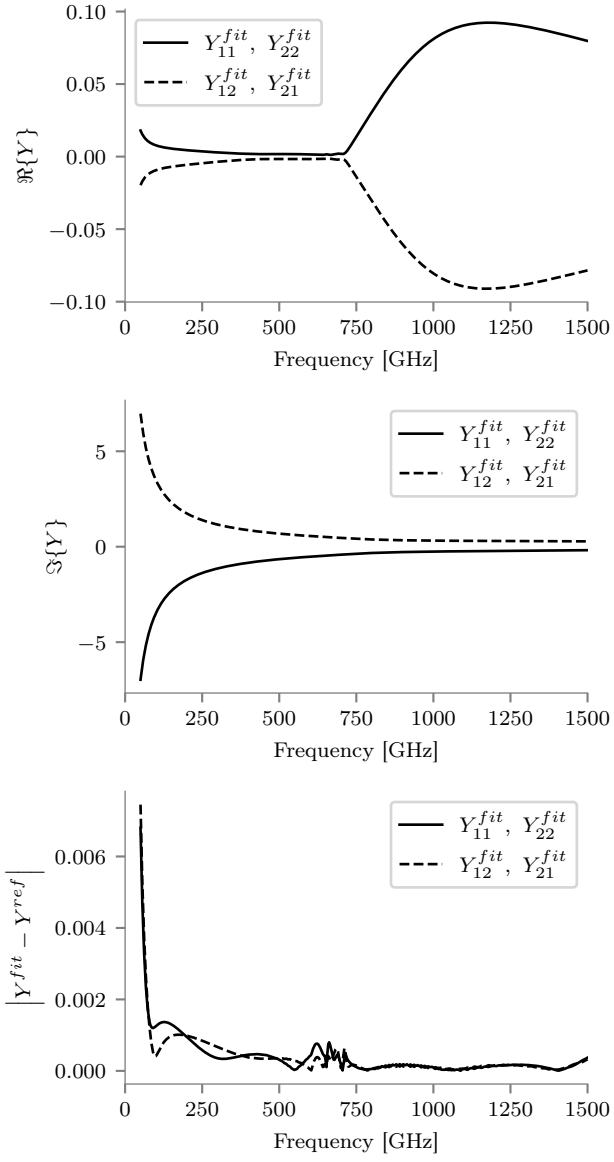

Figure 3.8: Approximated admittance of the 10 µm long PTL using Vector Fitting

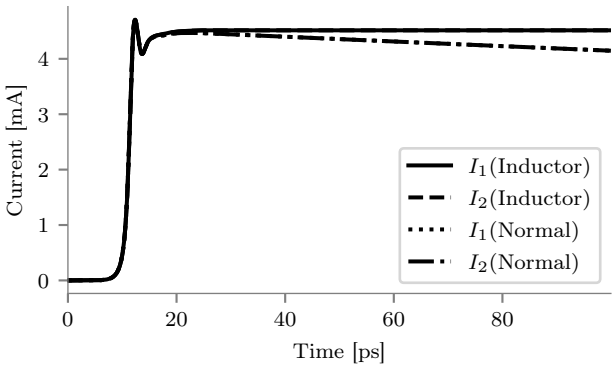

Figure 3.9: Vector Fitted approximation's response to the test waveform

	Admittance	Impedance
Basis Function Transformation	$\Phi(s) = \Phi'(s) + \frac{1}{sL}$	—
Non-superconducor response	$H'(s) = H(s) - \frac{1}{sL}$	—
Non-superconducor weighting	$w'(s) = w(s)$	—

Table 3.1: Superconductor subtraction

like a superconductor. For superconductor vector fitting the superconducting effect has to be exactly enforced.

3.6.2 Superconductor modification

Superconductor Vector Fitting is any vector fitting algorithm which exactly enforces (3.73) and (3.76) for admittance, (3.74) and (3.77) for impedance, and (3.75) and (3.78) for S-parameters.

We propose two methods to enforce superconductivity exactly: Superconductor subtraction, and Superconductor factoring. The S-parameter superconductor constraints add coupling between the different matrix entries. This prevents the speed-up of the fast variant of the vector fitting algorithm. We will, therefore, not investigate superconductor vector fitting applied to scattering-parameters. Not due to the difficulty in implementation or formulation, but simply because the admittance and impedance fitting is computationally an order of magnitude less expensive.

Superconductor subtraction is when the superconductor effect is subtracted from the superconductor response. The modified response is then fitted using standard vector fitting algorithms. The superconductor effect is then added back to the fitting response to get back the superconductor response. This is equivalent to having the superconductor network attached to the non-superconductor fitted network in parallel. Superconductor subtraction is only possible with Admittance parameters as the Impedance requires a numerical zero which is not possible to obtain using a linear transform. The modifications necessary are described in Table 3.1.

Superconductor factoring is when the superconductor effect is factored from the

	Admittance	Impedance
Basis Function Transformation	$\Phi(s) = \frac{\Phi'(s)}{s}$	$\Phi(s) = s\Phi`(s)$
Non-superconducor response	$H'(s) = sH(s)$	$H'(s) = \frac{H(s)}{s}$
Non-superconducor weighting	$w'(s) = \frac{w(s)}{s}$	$w'(s) = sw(s)$

Table 3.2: Superconductor factoring

Figure 3.10: Approximated admittance of the 10 µm long PTL using Superconductor Vector Fitting

superconductor response. The modified response is then fitted using standard vector fitting algorithms. The superconductor factor is then multiplied into the fitted response to get back the superconductor response. This is equivalent to having the superconductor effect added through a series state-space transformation on the non-superconductor network. The modifications necessary are described in Table 3.2.

The above weighting adjustments are neccesary so that the weighting of the original problem is not adjusted. The vector fitting transformation are derived in Appendix G. When the exact DC response of the system is known, we recommend fitting the Admittance using superconductor extraction as this DC response can be exactly enforced. When the DC response is not known, we recommend superconductor factoring as the DC response is then fitted in the least-squares sense.

3.6.3 Results

We implemented the superconductor modification to our programme and determined an improved model which obeys the superconductor constraints. In our PTL model we know the DC inductance exactly so we used the superconductor subtraction method. We fitted the 10 µm long PTL response again and the fitted admittance is shown in Fig. 3.10.

The model was converted to JoSIM format and tested with the test signal. The current response is plotted in Fig. 3.11.

The approximated admittance is still excellently fitted using six complex pole

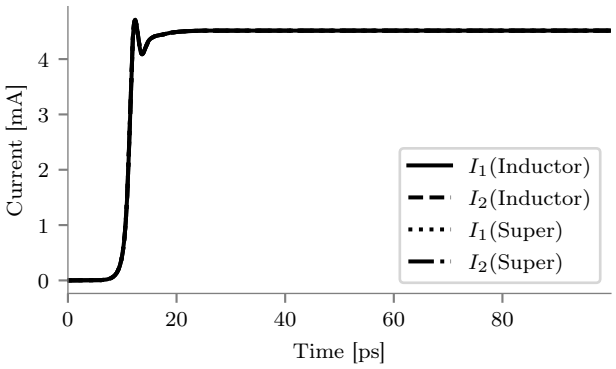

Figure 3.11: Superconductor Vector Fitted approximation's response to the test waveform

pairs. The current response to the test signal correctly exchibits expected low-frequency characteristics.

With the superconductor vector fitting, we now move on to fitting a moderately sized 1 mm long PTL.

Superconductor vector fitting was applied to the admittance of the 1 mm long PTL using 32 initial complex pole pairs. The fitted admittance is shown in Fig. 3.13.

Even with the resonances on the PTL the fit remains excellent.

3.7 Modality

The superconductor vector fitted PTL, again, looks correct, but if the model where to be terminated by an open circuit and driven by a voltage source the result would not be close to the expected response. The response is expected to give the impedance parameters of the PTL, as shown in Fig. 3.14, but instead the very wrong response, as shown in Fig. 3.15, is obtained.

The reason for this error is because the error of the admittance parameters is minimized with no regard for the eigenvalues of the admittance parameters. If the admittance parameters contain both small and large eigenvalues, the small eigenvalues are given a relatively small weighting in the fitting problem. The impedance parameters are the inverted admittance parameters. The small eigenvalues of the admittance parameters become the large eigenvalues of the impedance parameters. The error in the small eigenvalues is magnified, which is what caused the massive error in the fitted response. The eigenvalue value is error is calculated with $\left|\frac{eig(Y^{fit})-eig(Y^{ref})}{eig(Y^{ref})}\right|$. The eigenvalue error is shown in Fig. 3.16, and confirms and visualizes the problem.

This extreme error, up to 12500%, is unacceptable and needs to be corrected.

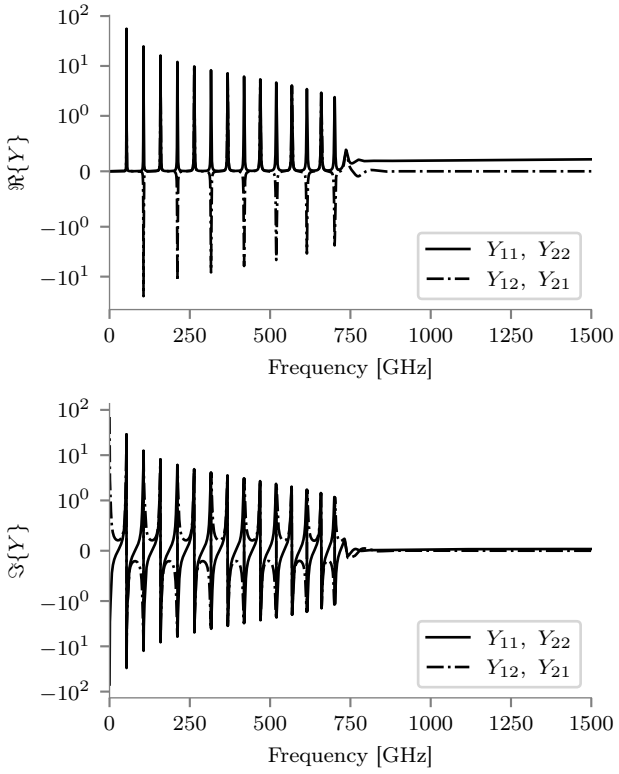

Figure 3.12: Admittance of the 1 mm long PTL

3.7.1 Projection

Vector Fitting where the eigenvalue error is minimized is called Modal Vector Fitting [47]. Instead of weighting the problem inversely proportional to the magnitude of the matrix entry, each matrix row is projected onto each eigenvector and weighted inversely proportional to the corresponding eigenvalue [47]. This results in the modal vector fitting weighting:

$$\frac{1}{|\lambda_i|}\left(\mathbf{H}^{fit}\cdot\mathbf{v}-\lambda_i\mathbf{v}_i\right)\approx 0. \tag{3.79}$$

The system of equations resulting from the modal weighting, (3.79), is significantly larger and denser than the original problem [47]. The fast vector fitting method can also not be utilized in its current form. There is a fast modal vector fitting algorithm, but it is still significantly slower than the conventional fast vector fitting algorithm [48].

For a general frequency-dependent network equivalent (FDNE) structure, this approach must be followed. However, for a two-port network, such as a PTL, a more straightforward solution exists.

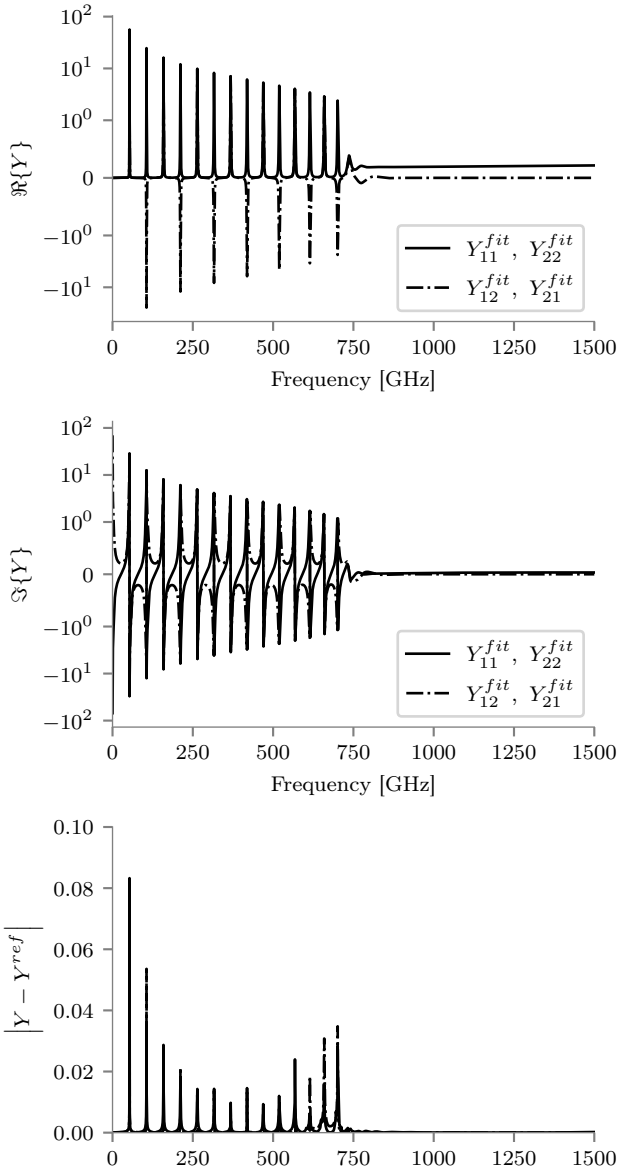

Figure 3.13: Approximated admittance of the 1 mm long PTL using Superconductor Vector Fitting

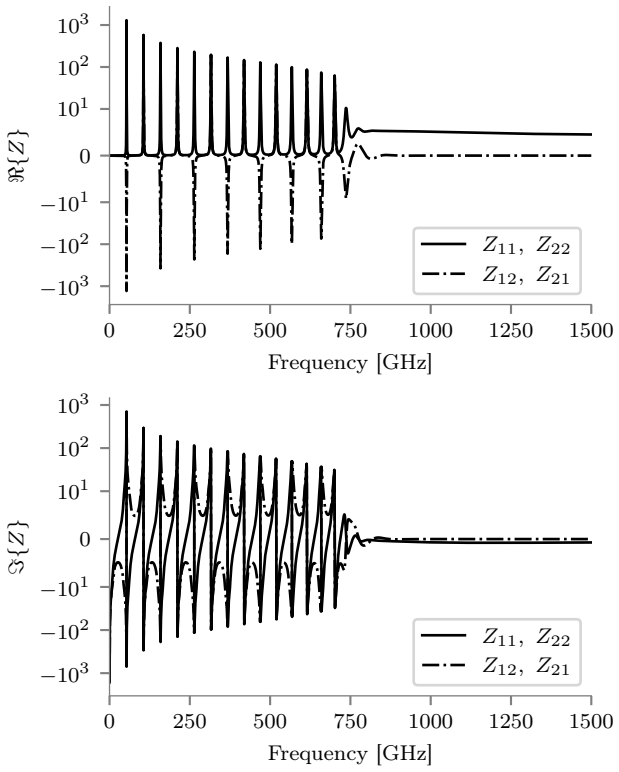

Figure 3.14: Reference PTL model impedance

3.7.2 Real Transform

The admittance matrix of a transmission line is symmetric and reciprocal. There exists a transformation matrix, $\mathbf{T}_2$, which diagonalizes all symetric and reciprocal 2x2 networks. The diagonalization process, and the transform matrix, $\mathbf{T}_2$, is shown in (3.80), and (3.81) respectively.

$$\mathbf{D} = \mathbf{T}^{-1} \cdot \mathbf{A} \cdot \mathbf{T} \tag{3.80}$$

$$\mathbf{T}_2 = \begin{bmatrix} -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{3.81}$$

The transformation matrix, $\mathbf{T}_2$, is symmetric, $\mathbf{T}_2 = \mathbf{T}_2^T$, and unitary, $\mathbf{T}_2^T = \mathbf{T}_2^{-1}$. The transform, if applied to a symmetric and reciprocal 2x2 network, results in

$$\mathbf{T}_2 \cdot \begin{bmatrix} A_{diag} & A_{off} \\ A_{off} & A_{diag} \end{bmatrix} \cdot \mathbf{T}_2 = \begin{bmatrix} A_{diag} - A_{off} & 0 \\ 0 & A_{off} + A_{diag} \end{bmatrix}. \tag{3.82}$$

Modal Vector Fitting can also be enforced by applying a constant real transformation matrix if a frequency-independent matrix can be found that diagonalizes

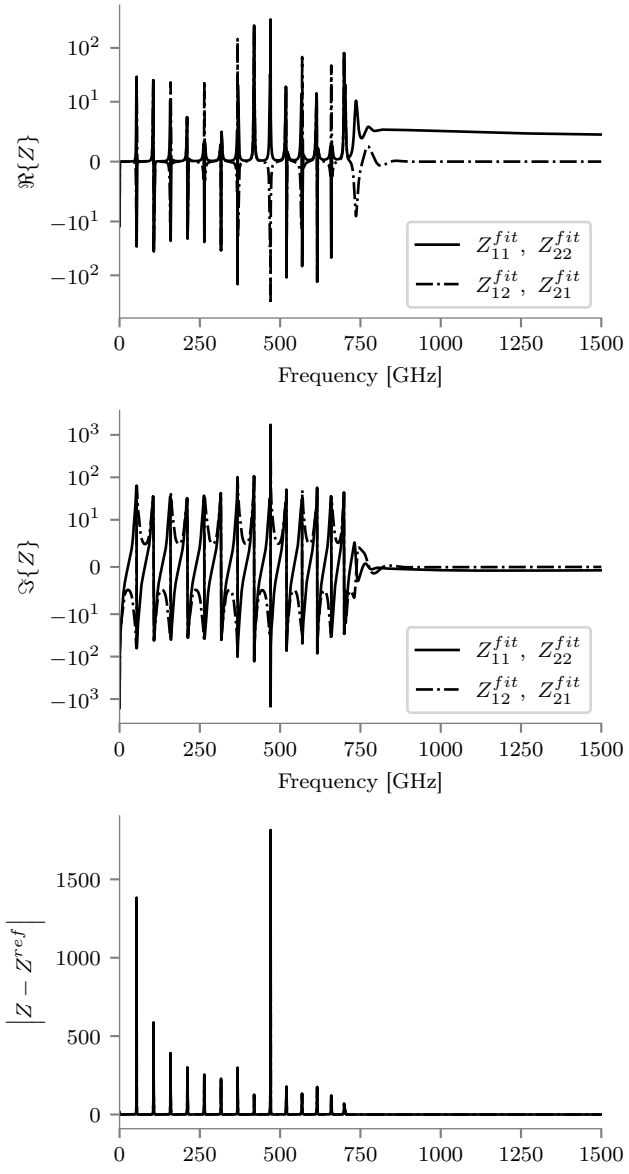

Figure 3.15: Superconductor Vector Fitted PTL model impedance

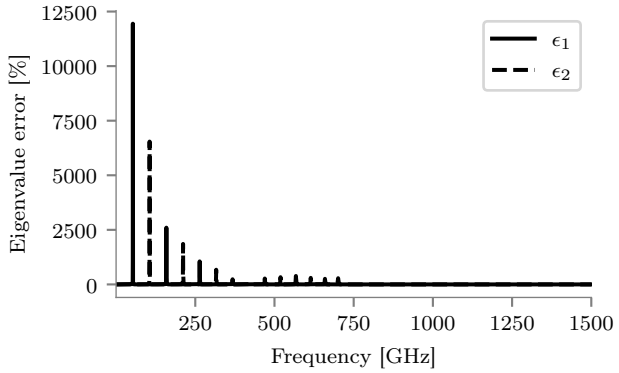

Figure 3.16: Eigenvalue error of the Superconductor Vector Fitted PTL model

the system. It was shown that such a matrix, $\mathbf{T}_2$, exists for all 2x2 symmetric and reciprocal networks. The procedure is therefore applicable for modelling the PTL.

3.7.3 Application

The PTL admittance parameters are diagonalized using the transformation matrix, $\mathbf{T}_2$ and symbolically simplified as shown in (3.83). The superconductor modification is made to the diagonalized PTL admittance and is shown in (3.84).

$$\mathbf{T}_2 \cdot \mathbf{Y}_{TL} \cdot \mathbf{T}_2 = \begin{bmatrix} \frac{1}{Z_L}\coth(\frac{\gamma l}{2}) & 0 \\ 0 & \frac{1}{Z_L}\tanh(\frac{\gamma l}{2}) \end{bmatrix} \tag{3.83}$$

$$\mathbf{T}_2 \cdot \mathbf{Y}_{TL} \cdot \mathbf{T}_2 = \begin{bmatrix} \frac{1}{Z_L}\coth(\frac{\gamma l}{2}) - \frac{2}{Z_L \gamma l} & 0 \\ 0 & \frac{1}{Z_L}\tanh(\frac{\gamma l}{2}) \end{bmatrix} \tag{3.84}$$

If we take the limit as the frequency goes to zero we get

$$\lim_{\omega \to 0} \left\{ \frac{1}{Z_L}\coth(\frac{\gamma l}{2}) - \frac{2}{Z_L \gamma l} \right\} = 0, \text{ and} \tag{3.85}$$

$$\lim_{\omega \to 0} \left\{ \frac{1}{Z_L}\tanh(\frac{\gamma l}{2}) \right\} = 0. \tag{3.86}$$

Since $\coth(\frac{\gamma l}{2})$ goes to infinity $\tanh(\frac{\gamma l}{2})$ necessarily goes to zero. The terms should be weighted inversely proportional to the eigenvalues and in this case, the diagonalized PTL admittance. The coth term would be weighted inversely to the unmodified term, but the tanh term should, therefore, be weighted inversely proportional to a term that goes to zero. It is, therefore, necessary to analytically enforce the zero of the system and simultaneously reweight the system to make the problem numerically feasible. The superconductor vector modification that enforces the impedance to go to zero can be used. It both enforces a zero at the origin and the reweighted problem does not have an infinite weight.

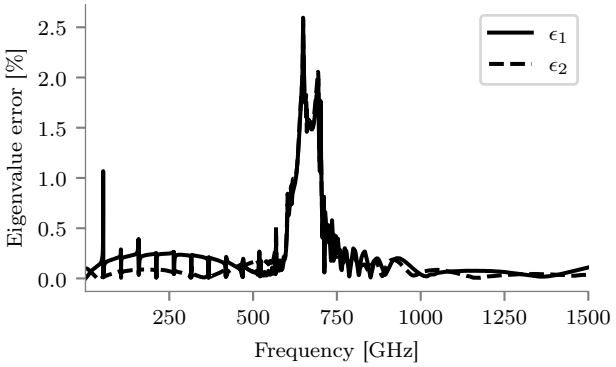

Figure 3.17: Eigenvalue error of Superconductor Modal Vector Fitted PTL model

3.7.4 Results

We implemented the modal modification to our program and determined an improved model which enforces modal accuracy. The fit was, again, performed using 32 complex pole pairs as starting poles. The eigenvalue error is plotted in Fig. 3.17.

We can see that the error is significantly lower and resembles the error of a usable model. Most of the error is situated around the gap frequency. This makes intuitive sense as the sharp discontinuity of the derivative cannot be exactly approximated by rational functions. Fortunately, very little of the energy of an SFQ pulse is situated in that region. The second most error is situated at the first resonance peak. This is the effective limiting error of the model. The error can be further reduced by increasing the pole count or increasing the weight around the area of interest, but for our study, it is not necessary.

To ensure that a small eigenvalue error corresponds to accurate admittance and impedance parameters, we plotted the admittance and impedance parameters in Fig. 3.18, and Fig. 3.19 respectively.

From the admittance and impedance parameter plot, we can see that both parameters are accurately represented.

3.8 Passivity

The modally accurate superconductor vector fitted PTL, again, looks accurate, but if the model is used in a unity feedback loop, the response will continue to increase until the simulation engine terminates. The PTL model is clearly not passive, and a unity feedback loop will continuously add energy to the system. For a system to be passive, the eigenvalues of the conductance should be positive.

$$eig(\Re\{\mathbf{Y}\}) >= \mathbf{0} \tag{3.87}$$

To confirm that our model is indeed non-passive the conductance of the modal superconductor PTL model is plotted in Fig. 3.20. We can clearly see that the

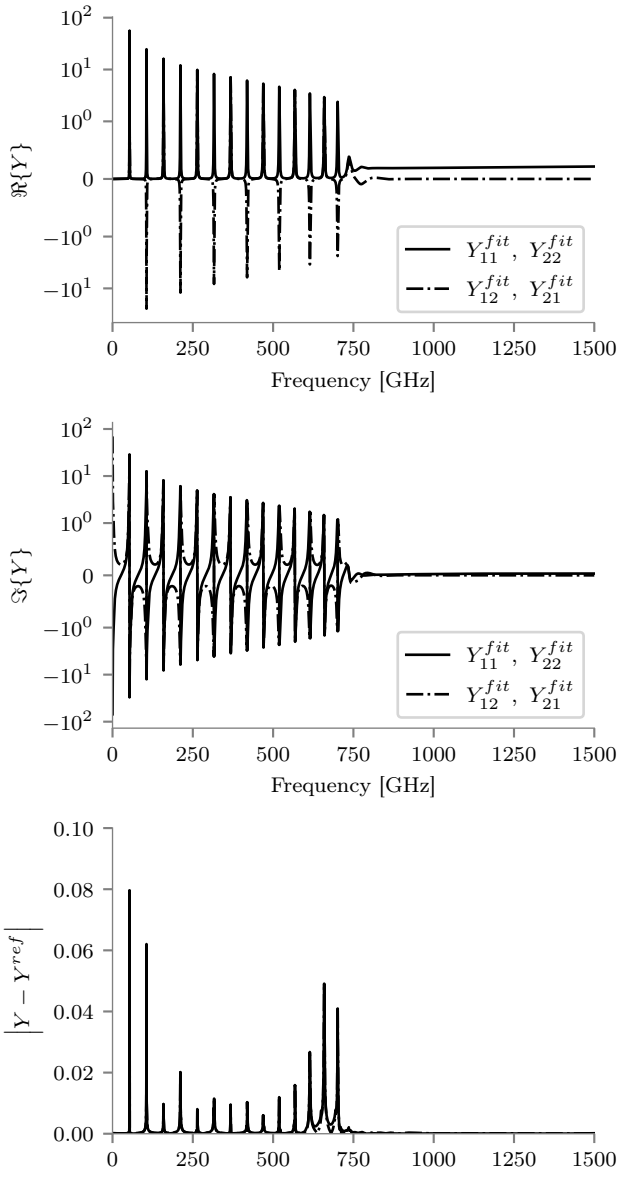

Figure 3.18: Superconductor Modal Vector Fitted PTL model admittance

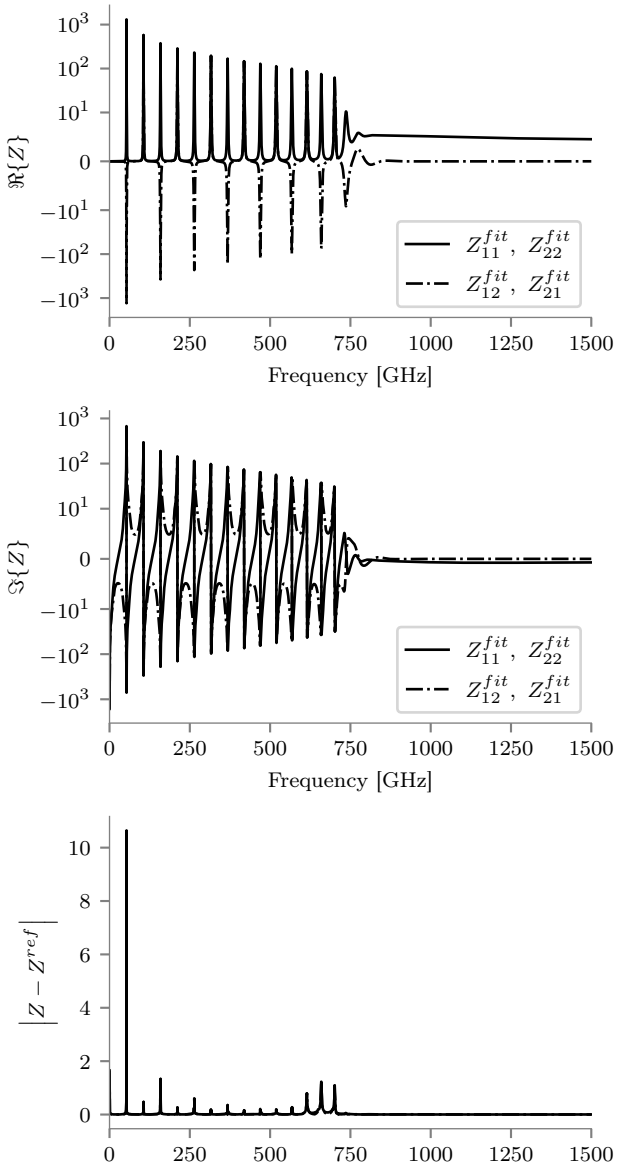

Figure 3.19: Superconductor Modal Vector Fitted PTL model impedance

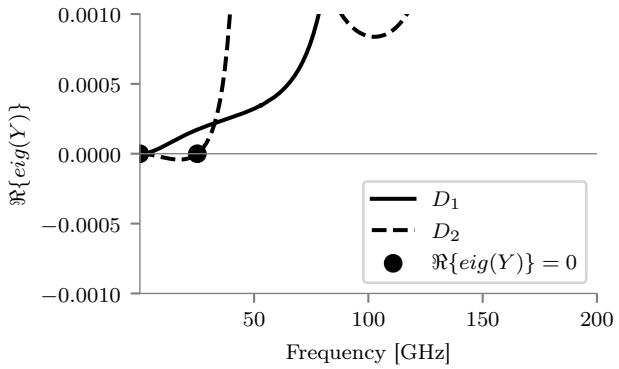

Figure 3.20: Superconductor Modal Vector Fitted PTL conductance eigenvalues

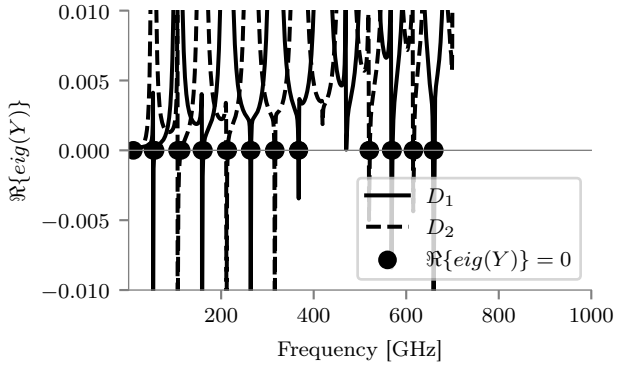

Figure 3.21: Superconductor Vector Fitted PTL conductance eigenvalues

conductance drops below zero. This is a small passivity violation, but a passivity violation none the less. It is pure coincidence that the violation is so small. If we inspect the non-modal model for passivity, shown in Fig. 3.21 we see that the situation is much worse.

The standard passivity enforcement techniques that are used in standard vector fitting can be directly applied to the modal superconductor vector fitting algorithm. The numerical procedure will be explained.

3.8.1 Residue perturbation

Many methods exist for passivity enforcement [52; 53; 54; 55]. Due to its effectiveness, we will use residue perturbation to passivate the PTL model. A constraint is added to ensure that the eigenvalues of the conductance are positive [52]. This results in the constrained least squares problem shown in (3.88).

$$\begin{aligned} \mathbf{w\Phi x} &\approx \mathbf{wH} \\ eig(\mathbf{G(x)}) &>= 0 \end{aligned} \tag{3.88}$$

The conductance is enforced only at select violating frequencies to discretize the constraint. The violations are then iteratively updated after the constrained problem is solved. It is assumed that the changes required in the residues are small enough to linearize the effect the residues have on the conductance eigenvalues. This makes $eig(\mathbf{G(x)}) >= 0$ a set of linear inequality constraints.

For the PTL or any model that has a constant real transformation matrix, the passivation can be individually applied to each diagonal entry. This results in the simplified constrained least-squares problem shown in (3.89).

$$\begin{aligned} \mathbf{w\Phi x}_{\lambda_i} &\approx \mathbf{wH}_{\lambda_i} \\ \Re\{\mathbf{w\Phi}_c\}\mathbf{x}_{\lambda_i} &>= 0 \end{aligned} \tag{3.89}$$

The simplified passivity enforcement does not require the eigenvalues of the conductivity to be linearized as the system is already linear.

3.8.2 Optimal constraining frequencies

To minimize the number of constraints, and to not let bands of violation persist in our model, we need a way of determining in what frequency bands our model becomes passive. Sampling the model over a wide frequency range is impractical as violations outside the sampling frequency can be missed [56]. To determe where the model might become passive one must first calculate $eig(\Re\{\mathbf{Y}\}) = 0$ [56] . For symmetric admittance models, such as our PTL, the crossing points of $eig(\Re\{\mathbf{Y}\})$ can be determined by computing the purely imaginary eigenvalues of the half-size singular admittance test matrix shown in (3.90) [56].

$$\mathbf{S} = \mathbf{A}(\mathbf{BD}^{-1}\mathbf{C} - \mathbf{A}). \tag{3.90}$$

After determining all the crossing points from the half-size singular test matrix, one should determine which bands are frequency violations bands. The midpoint of all the bands, any point before the first crossing and any point after the last crossing is sampled to determine which bands are causing passivity violations. From within each band, the point of maximum passivity violation can be determined through any numerical technique. The constraining frequencies do not need to coincide with the points of maximum passivity violations and can even be centre points of the band. However, choosing the constraining frequencies to coincide with the maximum passivity violation does reduce the number of passive correction iterations.

3.8.3 Quadratic programming

After determining the frequency points at which passivity should be explicitly enforced, we can proceed with the numerical implementation. Unfortunately, the constrained linear least-squares problem is significantly more challenging to solve than

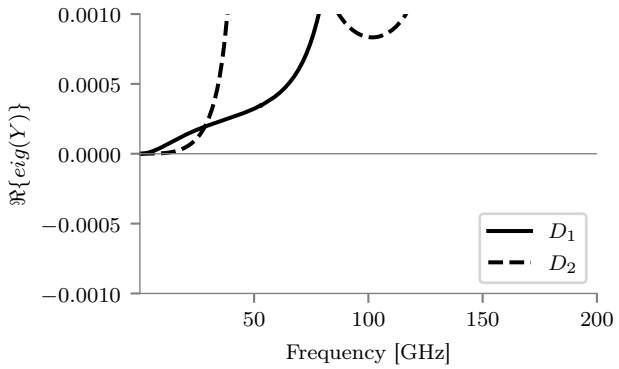

Figure 3.22: Passivated Superconductor Modal Vector Fitted PTL conductance eigenvalues

the standard linear least-squares problem. The problem has to be rephrased into a quadratic programming problem [57]. From [57], if the least squares problem is in the form

$$\begin{aligned} \mathbf{Ax} &\approx \mathbf{b} \\ \mathbf{Gx} &\leq \mathbf{h}' \end{aligned} \tag{3.91}$$

then

$$\frac{1}{2}\mathbf{x}^T\mathbf{A}^T\mathbf{Ax} - \mathbf{b}^T\mathbf{Ax} \tag{3.92}$$

should be minimized subject to

$$\mathbf{Gx} \leq \mathbf{h}. \tag{3.93}$$

The quadratic programming problem defined by (3.92), and (3.93) can be solved by any quadratic programming solver. We used cvxopt [58] to solve the quadratic programming equivalent of the constrained least squares problem, (3.89).

3.8.4 Results

We implemented the passivity enforcement with residue perturbation to our program and determined a passive model which still enforces modal accuracy. The fit was, again, performed using 32 complex pole pairs as starting poles. The passive model only has $eig(\Re\{\mathbf{Y}\}) = 0$ at $\omega = 0$ and the model is never non-passive, $eig(\Re\{\mathbf{Y}\}) >= 0$. The plot showing the region of the previous passivity violation is shown in Fig. 3.22.

The change in residues from the non-passive to the passive model was minimal. The increase in error should be negligible. To ensure that that is indeed the case the eigenvalue error is shown in Fig. 3.23

The eigenvalue errors remain almost unchanged with the difference not visible in the visualisation.

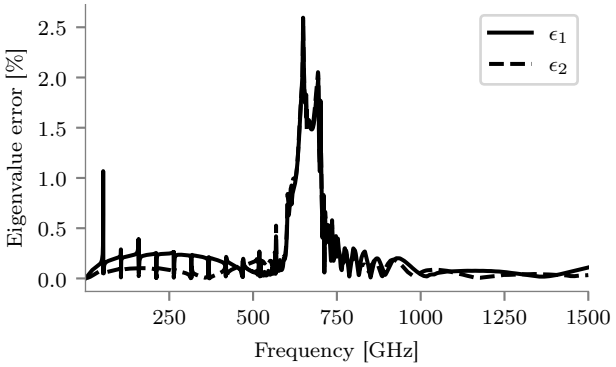

Figure 3.23: Eigenvalue error of the Passivated Superconductor Vector Fitted PTL model

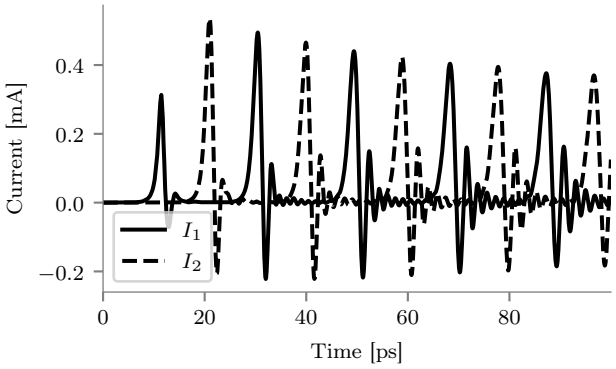

Figure 3.24: Passivated Superconductor Modal Vector Fitted PTL model short circuit response

3.9 Results

With a highly accurate and passive model for the PTL we can start investigating the time-domain response of PTLs.

3.9.1 Comparing the PTL with an ideal TL

In this test setup we connect one side of the PTL with a voltage source that generates a test signal and we test the responses with different loading conditions. We compare with an ideal PTL to see the difference that the more accurate model makes.

First, we test the short-circuit response. The short-circuit PTL response is shown in Fig. 3.24, and the short-circuit ideal TL response is shown in Fig. 3.25.

We can see that in the ideal case, the pulse shape remains unaffected. The pulse will perfectly reflect as long as the simulation keeps running. The pulse on the PTL starts spreading out, and its' peak decreases as time goes on. The PTL response

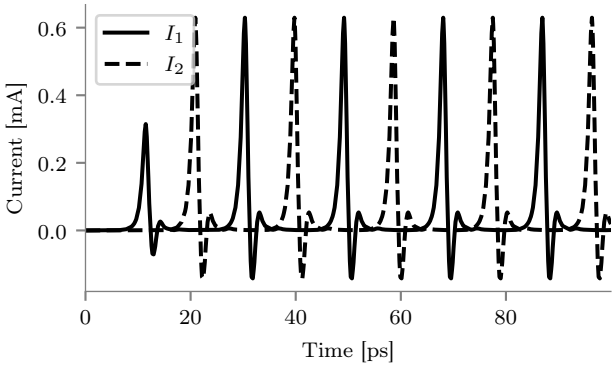

Figure 3.25: Ideal TL model short circuit response

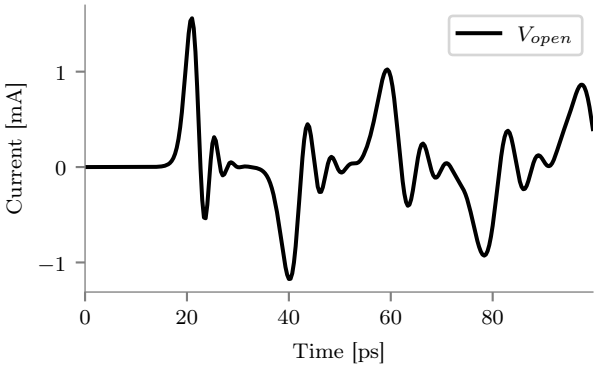

Figure 3.26: Passivated Superconductor Modal Vector Fitted PTL model open circuit response

also achieves a steady-state where the current is equal to $\frac{\Phi_0}{L_{PTL}}$.

Next, we test the open circuit response. The open-circuit PTL response is shown in Fig. 3.26, and the open-circuit ideal TL response is shown in Fig. 3.27.

Again, we can clearly see that in the ideal case the pulse shape remains unaffected. The pulse will, again, perfectly reflect as long as the simulation continues to run. Similarly, the pulse on the PTL starts spreading out and its' peak is decreasing as time goes on. This time the pulse achieves a steady state where there is no current flowing in the PTL.

3.9.2 Propagating pulse

It is clear that the pulse shape changes over time on a PTL. Next, the transformation of the pulse on an infinite PTL is studied. We simulate a finite PTL with a voltage source that generates the test signal and is shorted at the other end. To make sure

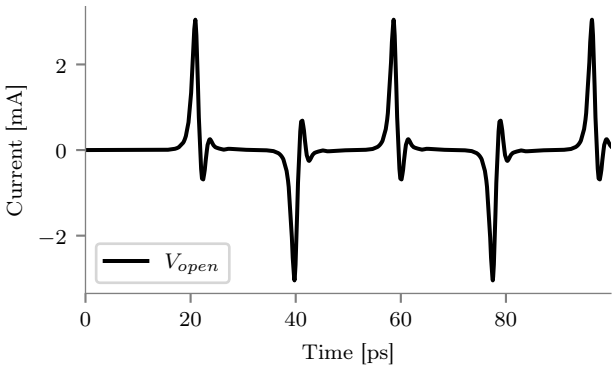

Figure 3.27: Ideal TL model open circuit response

we are looking at the forward pulse and not a reverse pulse, we simulated all signals with double the PTL length and sample the signal in the centre of the PTL. The voltage and phase along the line are shown in Fig 3.28.

We can see that the peak voltage drops, the pulse gets spread out, and it develops an oscillating tail. This pulse transformation is similar to measurements from a travelling wave on a superconductor co-planar transmission line [59]. The abnormal shape of the pulse arriving at a receiving circuit will influence how the receiving circuit responds to the pulse. The receiver circuit might reflect the elongated pulse if care is not taken.

Very interestingly, the phase does not decrease as the pulse travels. We can intuitively explain this from the superconductor phenomenon. By applying a voltage signal to the PTL we are forcing magnetic flux into the circuit. Due to the superconductor effect the magnetic flux cannot pass through the superconductor and must remain in the PTL. The losses in the PTL causes the magnetic wave to become elongated, but it does not dissipate it.

This unique characteristic is not immediately apparent without looking at the time-domain response. The flux conservation potentially makes it possible to propagate pulses across vast distances. Having an accurate PTL model is going to be critical in the design of long-distance PTL drivers and receivers.

3.9.3 Basic PTL driver and reciever

Finally, we test our PTL model in a simplified PTL driver and receiver. The driver and reciever are not designed for impedance matching and the junction model does not contain the usual parasitic elements. The test circuit is shown in Fig. 3.29.

The driver and receiver follow a simple design where all junctions have a critical current of 100 µA, all inductors have an inductance of 3.3 pH, and all current sources produce a current of 140 µA. The driver and receiver are designed to have the junctions biased to 0.7 I_c and the loop inductances are chosen such that $\tau_J = \tau_{LOOP}$, where τ_J is the Josephson time constant of the junction and τ_{LOOP} is the time constant of the inductance loop.

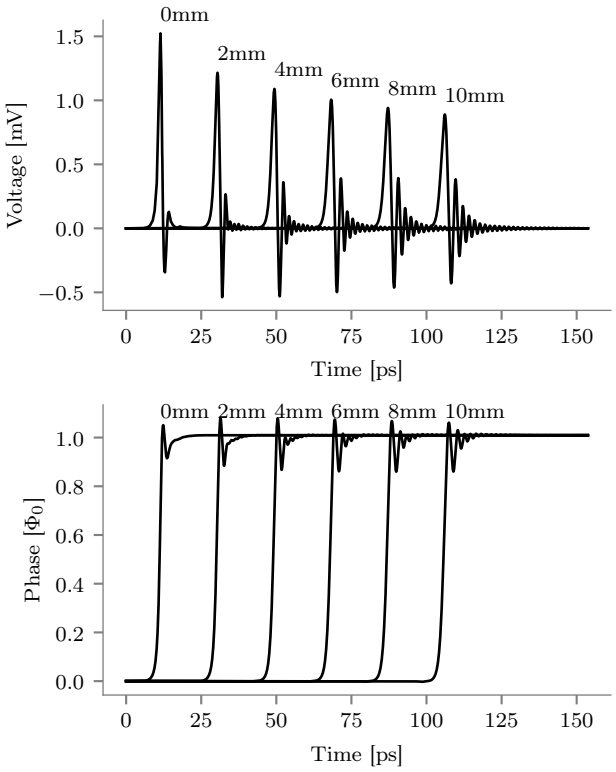

Figure 3.28: Travelling SFQ pulse along PTL

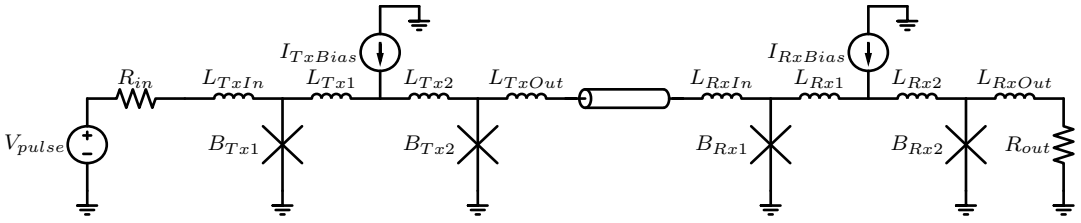

Figure 3.29: Basic PTL driver and reciever test setup

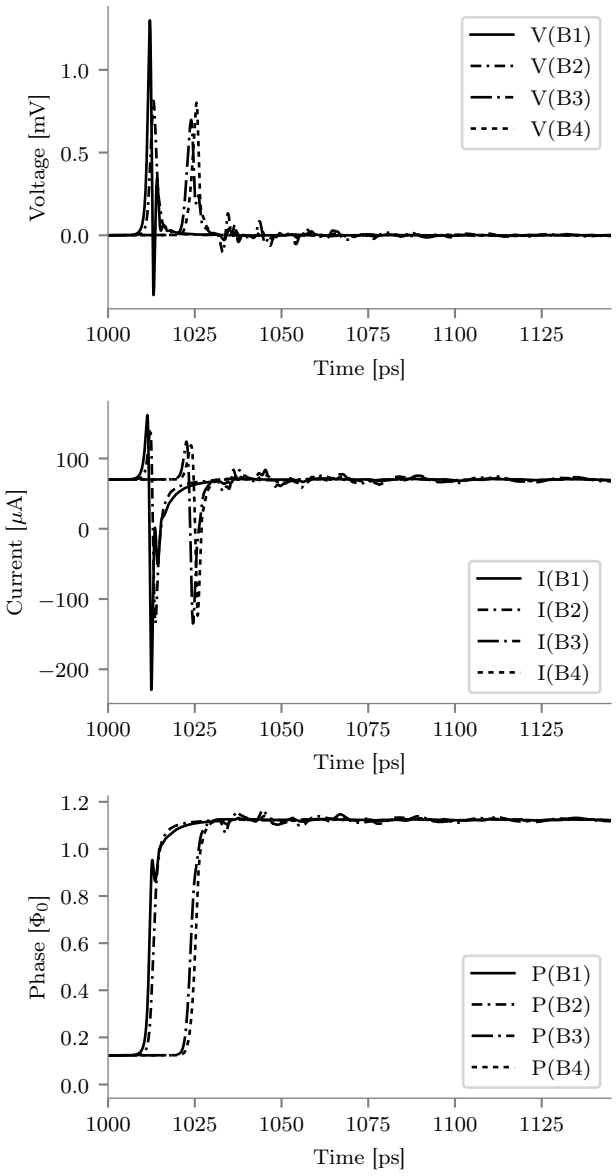

Figure 3.30: Basic 1 mm long PTL driver and reciever

The circuit first has to obtain a steady state before the test signal can be applied. For each 1 mm of PTL we wait 1 *ns* for the circuit to stabalize before sending the test signal. We tested the basic PTL driver and reciever with various PTL lengths. The responses of lengths, 1 mm, 1 cm, and 10 cm, are plotted in Fig. 3.30, Fig. 3.31, and 3.32 respectively.

The basic PTL driver and receiver works across long distances, but the reflections on the line will cause problems when the driver and receiver are operated at the lines resonance frequency.

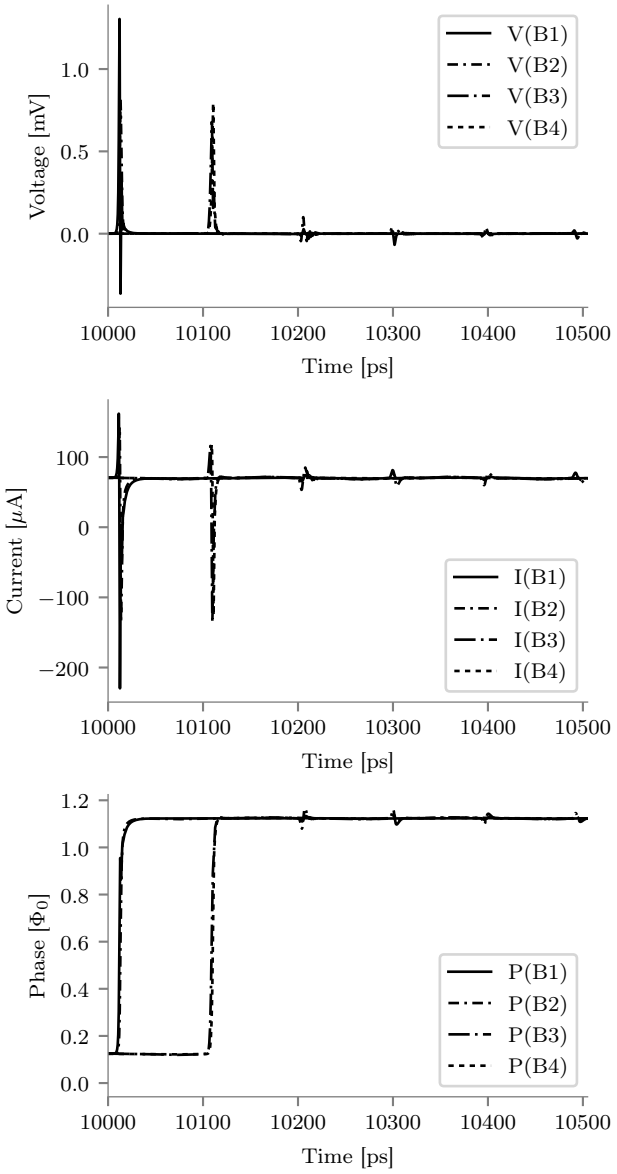

Figure 3.31: Basic 10 mm long PTL driver and reciever

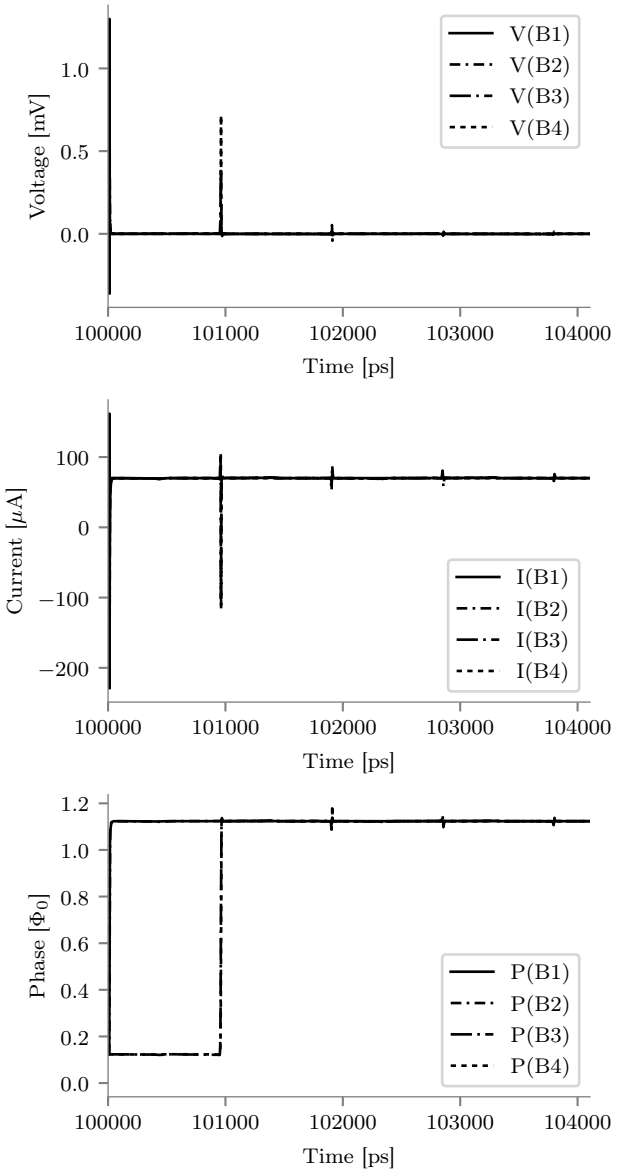

Figure 3.32: Basic 100 mm long PTL driver and reciever

3.10 Conclusion

3.10.1 Summary

Using Sanathanan-Koerner iteration, we fitted the admittance transfer function of a PTL. We chose our basis function to provide optimal numerical conditioning during the pole-relocation process and used a simplified basis function to reduce the number of elements in our state-space model. We had to adapt the iteration process to enforce the unique properties of the superconductor. Furthermore, care had to be taken to ensure that the transfer functions eigenvalues are kept accurate to ensure that the model is accurate under various loading conditions. The models' coefficients were perturbed to ensure that the model is passive and, therefore, stable in time-domain simulations.

Using the fitted model, we investigated the model in various loading conditions. We looked at how a pulse gets shaped as it propagates along a PTL. We finally used the PTL model in a PTL driver-receiver test setup to investigate the model.

3.10.2 Further improvements

- Superconductor Vector-Fitting can be extended to use time-domain basis functions in the case where only a time-domain signal is obtained. The requirements and transforms required for superconductivity have to be converted into time-domain.

- In long interconnects, such as the PTL, there is a time-delay in the circuit. Some optimizations can be made in cases where the ports are disconnected with a time-delay. Extending superconductor vector fitting to allow for delay components could significantly decrease the computational cost of the macromodels.

- In multi-port systems, the superconductor idealities have to be identified and enforced. If the frequency response comes from a 3D simulation, then the 3D simulation model could be used to detect the necessary superconductor modifications automatically.

3.10.3 Closing remarks

The insight that phase is conserved on a PTL is already immensely useful. It means it is possible to propagate SFQ pulses across vast distances. Using this technique to model superconductor interconnects will be very important in designing long-distance drivers and receivers.

The highly accurate model is, unfortunately, computationally expensive compared to the ideal transmission line. For shorter distances, it would be possible and recommended to use an ideal transmission in simulations. The exact distance at which the ideal transmission line model remains accurate depends on the use case of the PTL model.

Chapter 4

Yield Optimization

4.1 Introduction

Superconductor integrated circuits are becoming larger and more complex in an effort to scale these to challenge existing technologies. These Very Large Scale Integration (VLSI) circuits require robust circuit cells with very high fabrication yield. Circuit cells without a high fabrication yield will result in the inevitable failure of cells in a high-density design. High fabrication yield ensures there is a high probability of all cells working in a high-density design.

Numerous optimization methods exist, such as Inscribed Hyperspheres [60], Center of Gravity Method (CGM) [61; 62; 63], Single parameter optimizations and variations thereof [64; 65; 66; 67]. These methods produce circuits with suboptimal yield. Some of these methods also suffer from severe performance problems when scaling to higher dimensions. An improved yield optimization method is required when designing circuits for fabrication processes with high variance.

In this chapter, we develop a new yield optimization method specifically for SFQ logic circuits. The metric that is optimized is novel and statistically better than optimizing for critical margins. The optimizer is shown to be better than Cadence AAO [67], the current state of the art SFQ circuit optimizer.

4.2 Published Work

All relevant work, attached in Appendix B, is published in

- P. le Roux and C. J. Fourie, "**Distance-to-Failure-Maximization optimization algorithm for SFQ logic cells**," IEEE Trans. Appl. Supercond., vol. 30, no. 7, pp. 1-5, Oct. 2020.

4.3 Summary of research contributions

- Proposed a novel score function, the statistical distance to known points of failure, for circuit optimization. Maximizing the closest distance to failure produces a higher yield than maximizing the critical margin.

- An iterative optimization method, Distance-To-Failure-Maximization (DFM), was developed that retains information from previous iterations to improve the accuracy of the score function as the method progresses. The iterative method was shown to produce a circuit with a higher yield than the current state of the art SFQ optimizers, such as Cadence AAO [67].
- An open-source and freely available tool, josim-tools [68], was developed that implemented Distance-To-Failure-Maximization. The tool was used during the design of the Stellenbosch RSFQ cell library [69].

4.4 Conclusion

We presented a new optimization algorithm, the DFM method, that maximizes the closest distance to failure. This method improves on the current state of the art critical margin optimization. We have shown that the DFM method outperforms existing tools such as Cadence AAO. This method is extendable with the insights behind Cadence AAO localized optimization and global verification. This would allow optimizing large circuits effectively.

4.4.1 Closing remarks

Circuit dynamics are often strongly non-linear, and design equations often make many assumptions. Analytical solutions exist for simple circuits, but for circuits with numerically defined responses, such as PTLs, automatic optimization tools become essential in the circuit design process.

Chapter 5

Fundemental Inductance Model

5.1 Introduction

Inductances and Josephson junctions are the fundamental circuit elements in superconductor digital circuits. Accurate extraction and modelling of inductances are essential to the modelling and design of superconductor circuits. Any error in inductance extraction directly increases the error of the circuit model, where current distribution, switching dynamics and magnetic coupling are functions of inductance. This could lead to a circuit that works in simulation, but not when fabricated. Poorly modelled inductances are often the cause of circuit failure but are very seldom considered as the reason for failure. Other effects such as rogue flux trapping, bias current magnetic fields or local heating are often presented as the cause of circuit failure, but these are seldom validated.

In cases where mutual inductances are negligible, they can be safely ignored. Unfortunately, the assumption is seldom checked. We do an in-depth analysis of the extraction error when mutual inductance effects are ignored. The intuitive solution to the aforementioned problem is to add mutual coupling between all inductors. However, this leads to other problems. In a highly coupled netlist, the parameter extraction equations matrix is often ill-conditioned. This problem is also analyzed in depth.

In this chapter, we propose the fundamental inductance model which fully describes all kinetic and magnetic inductance effects. It does not suffer extraction from neglected inductances, and the extraction problem is not ill-posed. We apply the fundamental inductance model to various superconductor circuit designs in AQFP, RSFQ, and SQIFs. The importance of considering parasitic inductance in designs is highlighted. We conclude with the importance of using the fundamental inductance model during the design process.

5.2 Published Work

All relevant work, attached in Appendix C, is submitted for publication in

- P. le Roux, L. Schindler, and C. J. Fourie, "**Fundamental Inductance Modelling and its implications in superconductor circuit design**," IEEE

Trans. Appl. Supercond.

5.3 Summary of research contributions

- Two significant problems affecting inductance extraction, fitting errors and the singular value problem, was thoroughly analyzed. Fitting errors results from models without sufficient mutual coupling to describe the system. The singular value problem is caused by excessive mutual inductances which results in an undetermined system of equations and consequently a potentially non-physical least-squares solution.

- Propose the fundamental inductance model which include all inductive effects without numerical instability. Each fundamental inductor represents a fundamental cycle of the circuit graph. The self and mutual inductances correctly model all kinetic and magnetic inductance behaviour. How to determine self and mutual inductances of arbitrary loops from the fundamental

- An AQFP NOT gate was analyzed using the fundamental inductance model. It was shown that the 7% fitting error, from neglected mutual inductances, propagated to relevant circuit parameters. The equations of the circuit parameters were updated for the fundamental inductance model. The potential energy of the AQFP circuit was also derived for the fundamental inductance model. The new potential energy equations can be used to analyze the effect of asymmetries on the AQFP gate and reduce to the symmetric equation if symmetric substitutions are made.

- The inductance network of a PTL repeater, sometimes called a JTLT, was designed using the fundamental inductance model. The per-segment equivalent of the design was shown in the case where the parasitic couplings are negligible. The parasitic couplings are reduced to extractable circuit parameters. In the case where parasitic couplings are unavoidable, designing using the fundamental inductance model becomes a requirement instead of a convenience.

- The fitting error of a Superconductor Quantum Interference Filter (SQIF) was shown. The error was severe, and it clearly shows that the negligible coupling assumption made in designs are unfounded. The mutual coupling has to be taken into account to exploit the accuracy and wide dynamic range possible from the SQIFs. A more accurate inductance model, such as the fundamental inductance model, is required.

5.4 Conclusion

We have analyzed two significant causes of inductance extraction errors. We have shown that ignoring mutual inductance leads to incorrect self-inductances. We have also shown that adding too many inductors leads to exactly singular matrices during the extraction process. The Fundamental inductance representation was proposed,

which solves both the aforementioned problems. The effect of parasitic and asymmetric coupling on an AQFP gate was analyzed. How parasitics can influence RSFQ design was demonstrated through a loop-based design of a PTL repeater. We have shown that parasitic coupling introduces significant modelling errors in SQIFs. We conclude that the fundamental inductance model is essential in verifying superconductor circuits and designing circuits with parasitics.

5.4.1 Closing remarks

The fundamental inductance model does not only allow accurate modelling of inductive effects; it is also useful during superconductor circuit design. Design equations derived using the fundamental inductance model aids high-frequency SFQ design.

Chapter 6

Results: case study on JTLT design

6.1 Introduction

To demonstrate the developed methods and how the methods improve high-frequency SFQ design, we design a JTLT as an example. A JTLT is a JTL circuit with integrated PTL drivers and receivers. The example is not meant as a real-world design case-study. The example shows how all the work in this thesis ties together.

The JTLT circuit schematic, adapted from Appendix C, is shown in Fig. 6.1. The inductors of the bias branches are excluded as they do not have any influence when connected in series to a current source. The schematic does not include external PTL connections. The resistor, R_{out}, is a resistive break which prevents flux trapping and suppresses weak noise.

We design and optimize the circuit using the high-frequency characteristic impedance and PTL circuits. The JTLT should operate with sufficient margins, even when being driven at high frequencies. The JTLT should also sufficiently suppress weak noise so that it can be operated when driving a line at its resonance frequency.

We discuss our test setup and why design using equations are not sufficient for producing a high-frequency circuit. The junction's time constant peculiarities in the presence of connected PTLs and how they complicate equation-based-design are discussed.

We start our design from the design equation calculated using the Fundamental Inductance model. The initial design values are chosen based on existing works. The initial circuit is verified using a single pulse test. This tests that the circuit does not trap or reflect the incoming flux. The yield is then optimized using the simple verification procedure.

The simple verification procedure does not take into account any timing characteristic of the JTLT. For the JTLT to operate at high frequencies, the JTLT should sufficiently quickly pass along the fluxon and return to steady-state. Instead of directly optimizing timing constants, we optimize the yield of the circuit when tested using a high-frequency pulse train.

The high-frequency verification sufficiently reduces the response time of the

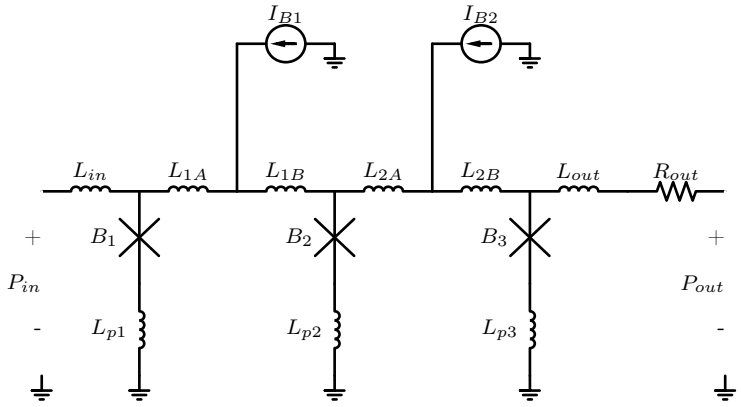

Figure 6.1: JTLT Schematic

JTLT, but it does not take into account any weak noise. We construct a JTLT-PTL-JTLT test setup which can be driven at various frequencies. We drive the testbench at the resonant frequency to determine circuit operation. The yield of the testbench is optimized to produce the final JTLT.

The case study concludes with a discussion and analysis of the final JTLT. We emphasize the improvements made by the numerical methods presented in this thesis.

6.2 Test setup

In some modern SFQ cell libraries [69] PTL drivers and receivers are integrated into cells. A resistive break between the circuits also prevents bias currents from leaking to adjacent cells. This allows cells to be designed in isolation and reduce the total number of junctions in a chip. The testbench, therefore, drives the device under test (DUT) from a PTL.

We are specifically interested in designing a high-frequency JTLT operating at a wide frequency range. Our testbench should, therefore, remain functional under various driving frequencies.

The traditional DCSFQ-PTLTX-JTLT-DUT-JTLT-PTLRX-SFQDC testbench is shown in Fig. 6.2. It generates a pulse by using a DCSFQ. The DCSFQ pulse sends the pulse on to a PTL driver (PTLTX). A JTLT circuit then shapes the pulse to provide a realistic driving pulse. The JTLT pulse is then sent on to the Device Under Test (DUT). Any pulses generated by the DUT is sent on to another JTLT, which represents a realistic receiving circuit. The JTLT then sends the pulse on to a PTL receiver (PTLRX). The PTLRX then connects with an SFQDC.

The traditional testbench has two problems which makes it unsuitable for our use case. The first is that we want to design a JTLT and we cannot have it as both a DUT and part of our testbench. The second, and more general, problem is that failures and noise of the testbench circuitry can cause the verification to fail

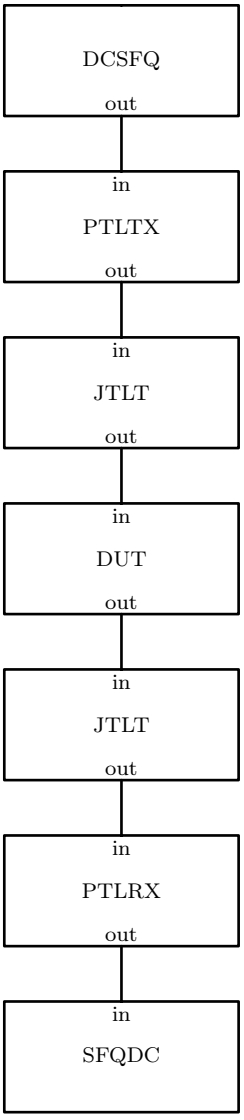

Figure 6.2: DCSFQ-PTLTX-JTLT-DUT-JTLT-PTLRX-SFQDC testbench setup

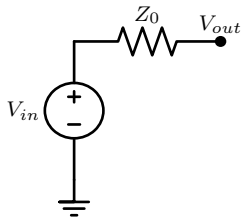

Figure 6.3: Infinite PTL Thevenin equivalent model

which prevents isolated testing of the DUT. For high-frequency operation a better testbench setup is required.

To avoid resonances at all frequencies, we need an infinitely long PTL connected to all the ports of the circuits. Reflections on the infinitely long PTL cannot influence our device under test. We can easily construct a Thevenin equivalent model using undergraduate transmission line theory. The equivalent infinite PTL model is shown in Fig. 6.3. It should be noted that the input voltage source should be double that of the desired forward wave.

This model does not limit us to ideal transmission lines. As long as we can find an element which is equivalent to the characteristic impedance, the equivalent circuit remains viable. We used the standard vector fitting algorithm with passivity enforcement to obtain an equivalent model of the characteristic impedance. Without loss of accuracy, we performed the fit with using the characteristic admittance as the resulting model is more efficient in SPICE. An accurate fit was obtained using eight complex starting poles. The frequency response of the fitted model is shown in Fig. 6.4

To verify that the resulting matching circuit matches our PTL model, we excited a PTL with the matching termination. The response is shown in Fig. 6.5. From the response, it is clear that the matching circuit absorbs the incoming pulse, and the reflected wave is negligible.

Using the Thevenin equivalent circuit of the PTL as sources and sinks for our testbench, we arrive at a minimal testbench, as shown in Fig. 6.6.

6.3 Design considerations

There are multiple aspects of design that need to be taken into account when designing and fabricating a circuit. We will not cover all design considerations as they are not relevant to the methods developed in this thesis. We will, however, clearly state what we intend to take into account and what we do not.

The timing characteristic of the circuit cannot be neglected as the JTLT should perform under high frequency. The characteristic impedance of the PTL and adjacent junction influences the junction's time-constants, which, in turn, affect the JTLT's timing characteristics. The shunt resistor of the junction not only influences the junctions timing characteristics it also influences the impedance matching of the

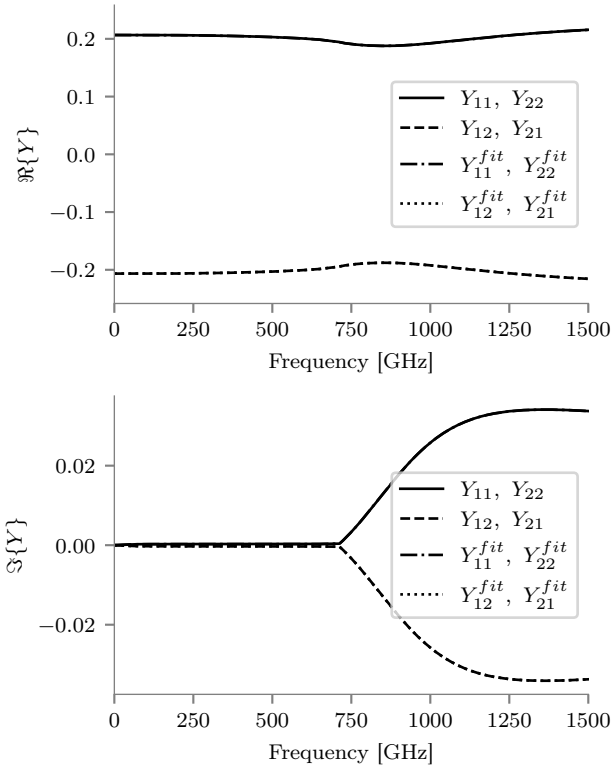

Figure 6.4: Characteristic addmitance reference and Vector Fitted model comparison

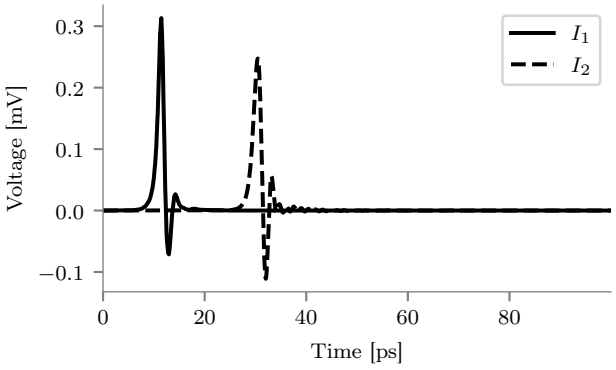

Figure 6.5: PTL matching impedance test

Figure 6.6: Simplified testbench

JTLT to the PTL. The shunt resistors are, therefore, allowed to vary during yield optimization.

The only form of noise we will take into account is the weak noise caused by the impedance and flux mismatch of the JTLT circuit. Other sources of noise are outside the scope of this dissertation. The bit-error-rate (BER) can be calculated and specified as a requirement. There are general methods to calculate the BER of RSFQ circuits [70]. We will, however, not take into account the BER, but we will limit the bias currents to 0.767 I_c. This ensures that the bias current can be increased by 30 % before the junction is over-biased. This prevents the optimizer from producing unrealistically high biased JTLT.

We will not optimize the JTLT for a specific process, and therefore, the layout will also not be taken into account. We will assume all our parameters are normally distributed and proportionally scaled to their nominal value. Process specific variation can be taken into account by using process-specific variation information. Since the optimizer operates on the schematic level, we also apply appropriate variable limits. The limits ensure that the optimizer does not produce variables that are too small or large to be fabricated.

The possible process variation of the PTL is not taken into account. We are already estimating material properties, and without more information on process variations, we cannot make sensible guesses as to estimate the effect of process variations. Consequently, we will also not go into the issue of PTL integration density, which is a higher-level and holistic consideration of SFQ cell library design.

Inter-cell variation is an important facet of SFQ cell library design. However, since this example is limited to only a JTLT, we will not take into account inter-cell variations.

The full variable list and boundaries of the design parameters are specified in Table 6.1. The design parameters, are not neccesarily the values of the circuit components, but rather the values that are used to calculate the circuit components.

The circuit parameters can be calculated from the design values by solving the design equations. See Appendix C for more details. The junction brances of Fig. 6.1 are simplified and include a shunt resistor with a parasitic shunt inductor. The circuit parameters include all the full list of parasitic components.

The solution to the design equations are listed in Table 6.2. The design equations are also dependent on several process parameters. I_{c0} is the critical current density, L_{sheet} is the inductance per µm^2, and R_{sheet} is the resistance per µm^2.

The full junction branch is shown in Fig. 6.7.

Design parameters	Lower bound	Upper bound
L_1	3.0 pH	8.0 pH
L_2	3.0 pH	8.0 pH
L_{in}	2.0 pH	2.0 pH
L_{out}	2.0 pH	2.0 pH
B_1	1.0 µm^2	2.5 µm^2
B_2	1.0 µm^2	2.5 µm^2
B_3	1.0 µm^2	2.5 µm^2
β_1	1.0	4.0
β_2	1.0	4.0
β_3	1.0	4.0
χ_1	0.3	0.767
χ_2	0.3	0.767
χ_3	0.3	0.767
R_{out}	1.21 Ω	4.838 Ω

Table 6.1: JTLT Design parameter boundaries

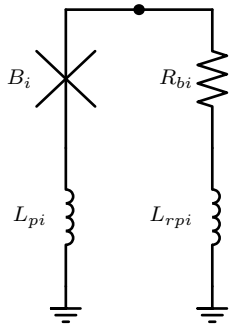

Figure 6.7: Full shunted junction schematic

Circuit parameters	Design Equations
L_{in}	2.0 pH
L_{out}	2.0 pH
L_{1A}	$-L_{p1} + \frac{\pi B_2 I_{c0} L_1 \chi_2 + \pi B_2 I_{c0} L_{p2} \chi_2 - \Phi_0 \operatorname{asin}(\chi_1) + \Phi_0 \operatorname{asin}(\chi_2)}{\pi(2B_1 I_{c0} \chi_1 + B_2 I_{c0} \chi_2)}$
L_{1B}	$L_1 - L_{p2} + \frac{-\pi B_2 I_{c0} L_1 \chi_2 - \pi B_2 I_{c0} L_{p2} \chi_2 + \Phi_0 \operatorname{asin}(\chi_1) - \Phi_0 \operatorname{asin}(\chi_2)}{\pi(2B_1 I_{c0} \chi_1 + B_2 I_{c0} \chi_2)}$
L_{2A}	$L_2 - L_{p2} + \frac{-\pi B_2 I_{c0} L_2 \chi_2 - \pi B_2 I_{c0} L_{p2} \chi_2 - \Phi_0 \operatorname{asin}(\chi_2) + \Phi_0 \operatorname{asin}(\chi_3)}{\pi(B_2 I_{c0} \chi_2 + 2B_3 I_{c0} \chi_3)}$
L_{2B}	$-L_{p3} + \frac{\pi B_2 I_{c0} L_2 \chi_2 + \pi B_2 I_{c0} L_{p2} \chi_2 + \Phi_0 \operatorname{asin}(\chi_2) - \Phi_0 \operatorname{asin}(\chi_3)}{\pi(B_2 I_{c0} \chi_2 + 2B_3 I_{c0} \chi_3)}$
L_{p1}	0.2 pH
L_{p2}	0.2 pH
L_{p3}	0.2 pH
L_{rp1}	$0.2\,\text{pH} + R_{b1} \times \frac{L_{sheet}}{R_{sheet}}$
L_{rp1}	$0.2\,\text{pH} + R_{b2} \times \frac{L_{sheet}}{R_{sheet}}$
L_{rp1}	$0.2\,\text{pH} + R_{b3} \times \frac{L_{sheet}}{R_{sheet}}$
R_{b1}	$\frac{1}{B_1} \times \sqrt{\frac{\Phi_0 \beta_1}{2\pi c_j i_c}}$
R_{b2}	$\frac{1}{B_2} \times \sqrt{\frac{\Phi_0 \beta_2}{2\pi c_j i_c}}$
R_{b3}	$\frac{1}{B_3} \times \sqrt{\frac{\Phi_0 \beta_3}{2\pi c_j i_c}}$
I_{bias1}	$I_{c0}\left(\chi_1 B_1 + \frac{\chi_2 B_2}{2}\right)$
I_{bias2}	$I_{c0}\left(\chi_3 B_3 + \frac{\chi_2 B_2}{2}\right)$
R_{out}	R_{out}
B_1	B_1
B_2	B_2
B_3	B_2

Table 6.2: JTLT Solution to Design Equations

6.4 Initial JTLT optimization

We are going to use the basic design equations derived in Appendix C. The initial design is taken from the Stellenbosch University RSFQ cell library [69].

The design parameters and their initial values are given in Table 6.3. We use the notation that β_i, and χ_i is the Stewart-McCumber parameter and bias ratio of junction i, respectively. The Stewart-McCumber is used to calculate the value of the resistor and the parasitic shunt inductance.

Before starting to optimize for high frequency and resonance, we first establish a simple verification procedure. A single pulse is sent to the JTLT as input. The JTLT is seen as working if the JTLT then transmits a single pulse from the output. The basic circuit operation is shown in Fig. 6.8. We take the output pulse and feed it back into the JTLT so that we ensure that the output is also large enough to trigger the next JTLT stage.

The margin analysis of the initial circuit parameters are shown in Fig. 6.9. The critical margin is I_{bias1} at 18.3%.

Design parameters	Initial values
L_1	6.462 pH
L_2	5.17 pH
L_{in}	2.0 pH
L_{out}	2.0 pH
B_1	1.6 µm^2
B_2	2.0 µm^2
B_3	2.5 µm^2
β_1	1.0
β_2	1.0
β_3	1.0
χ_1	0.7
χ_2	0.7
χ_3	0.7
R_{out}	1.36 Ω

Table 6.3: Initial JTLT Design parameters

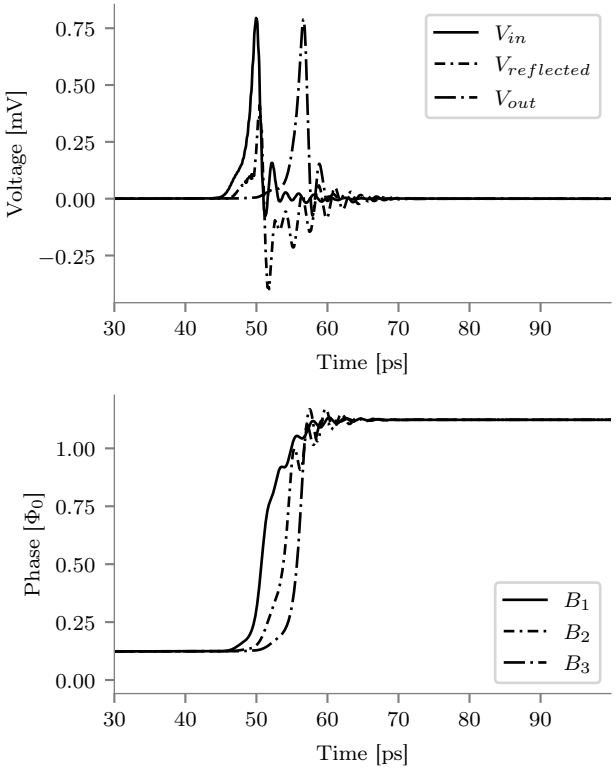

Figure 6.8: Simulation of initial JTLT

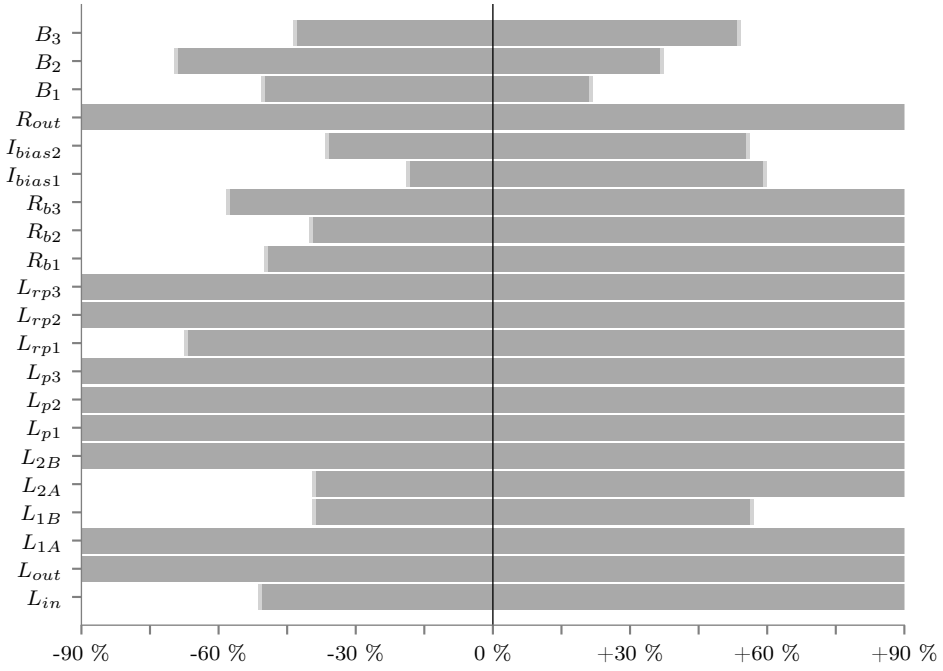

Figure 6.9: Initial JTLT basic margins

We must note that the cell library uses a different characteristic impedance than the line we are using in this study. The poor margins is not a reflection on the RSFQ cell library, but merely a consequence of our hypothetical test setup.

The JTLT is optimized for yield. The josim-tools optimization engine was used to optimize the circuit. The optimized parameters and margins of the optimized circuit is shown in Table 6.4 and Fig. 6.10.

The critical margin is the I_{bias1} current source at 51.3%. However, other failures are equally critical but do not lie on the individual parameter variation lines. If we were only optimizing for critical margin instead of closest point of failures, the closest failure, and therefore, the yield would be lower.

It can be seen that the junction areas are reduced to almost the minimum design boundary. The reduction in junction critical currents leads to an increase in shunt resistor size. The increase in shunt resistor size will improve the matching between the JTLT and the transmission line. To not have the optimizer reduce the junctions to such an extent, more restricted parameters need to be given to the optimizer or a more holistic verification function should be used. As previously stated, a more holistic verification function is outside the scope of this dissertation, and we will continue with the verification and design boundaries.

The simulation of the basic optimized JTLT is shown in Fig. 6.11.

We note that the initial pulse reflects very little energy showing a good impedance match between the PTL and the JTLT, but after the junction switches the dynamic behaviour of the circuit causes reflections. We cannot find a description of the

Design parameters	Initial values
L_1	7.528 pH
L_2	7.877 pH
L_{in}	2.0 pH
L_{out}	2.0 pH
B_1	1.014 µm^2
B_2	1.002 µm^2
B_3	1.015 µm^2
β_1	2.278
β_2	1.632
β_3	3.039
χ_1	0.6914
χ_2	0.4259
χ_3	0.5072
R_{out}	1.214 Ω

Table 6.4: Basic optimized JTLT design parameters

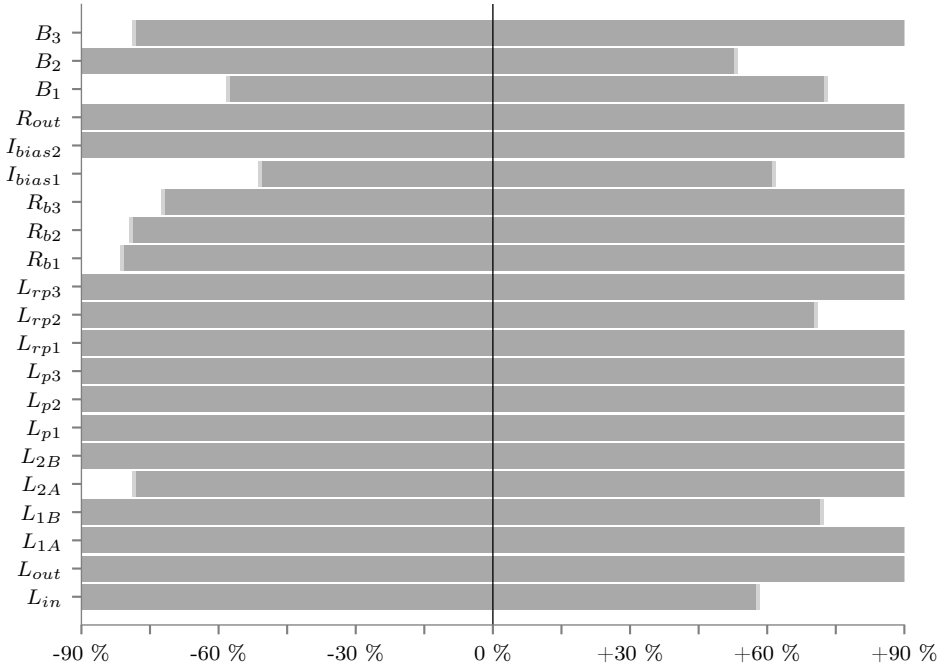

Figure 6.10: Basic optimized JTLT basic margins

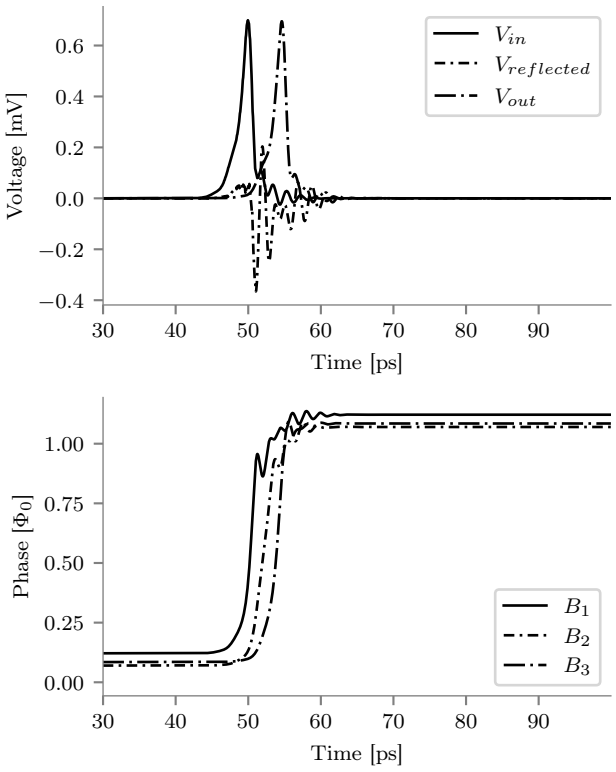

Figure 6.11: Simulation of basic optimized JTLT

phenomena in literature, so we will briefly explain what is happening. The pulse arriving at the junction is only a partial fluxon. It is partial since some of the magnetic fields escaped out of the output resistor branch of the previous JTLT stage. The junction, however, can receive enough energy to start switching from a partial fluxon, but for it to close the flux in superconductor loops has to be quantized. Therefore, if $\alpha\Phi_0$ arrives at the junction and the junction switches it can either reflect that $\alpha\Phi_0$ flux or it can let through an entire fluxon and reflect $(\alpha - 1)\Phi_0$ flux.

6.5 High speed JTLT optimization

With the basic optimized JTLT, we can start increasing the verification requirements. We aim for an operating frequency of 100 GHz. To ensure that the JTLT operates at such a high frequency, we test the JTLT at the desired frequency with a random data sequence. The simulation result of the basic optimized JTLT with the test sequence is shown in Fig. 6.12.

The high-speed simulation passes verification if all fluxon passes through the JTLT within 10 ps. With the high-speed verification procedure, we can perform a high-speed margin analysis of our basic optimized circuit.

The margin analysis is shown in Fig. 6.13. The critical margin is 40.8 %, but

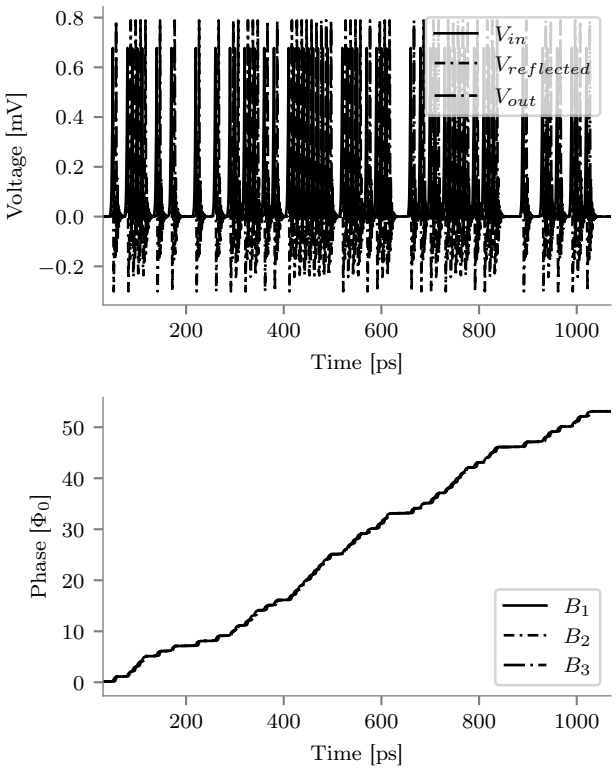

Figure 6.12: High speed simulation of basic optimized JTLT

three closer global failure can be easily found. The closest global failure is 35.5 % away.

Using the high-speed verification procedure and the basic optimized circuit as a starting point, we optimized the JTLT. The high speed optimized design parameters are shown in Table 6.5.

The margin analysis of the high-speed optimized circuit is shown in Fig. 6.14. The critical margin is 54.8 %, but the closest failure is 48.5 %, and three other failure points closer than the critical margin were also found.

The optimality of the high-speed circuit appears to be limited by the minimum junction size we specified as a parameter bound. As stated previously, since a holistic verification function is outside the scope of this dissertation, and we will leave the bounds and verification function as is.

6.6 Resonant JTLT optimization

With the high speed optimized JTLT, we can start optimizing the JTLT to work when the line has potential resonance. Instead of testing with a single JTLT, we now test with a JTLT-PTL-JTLT. In our test the PTL line segment is 3 mm. This allows us to drive the system at the resonance frequency of the PTL. The simulation

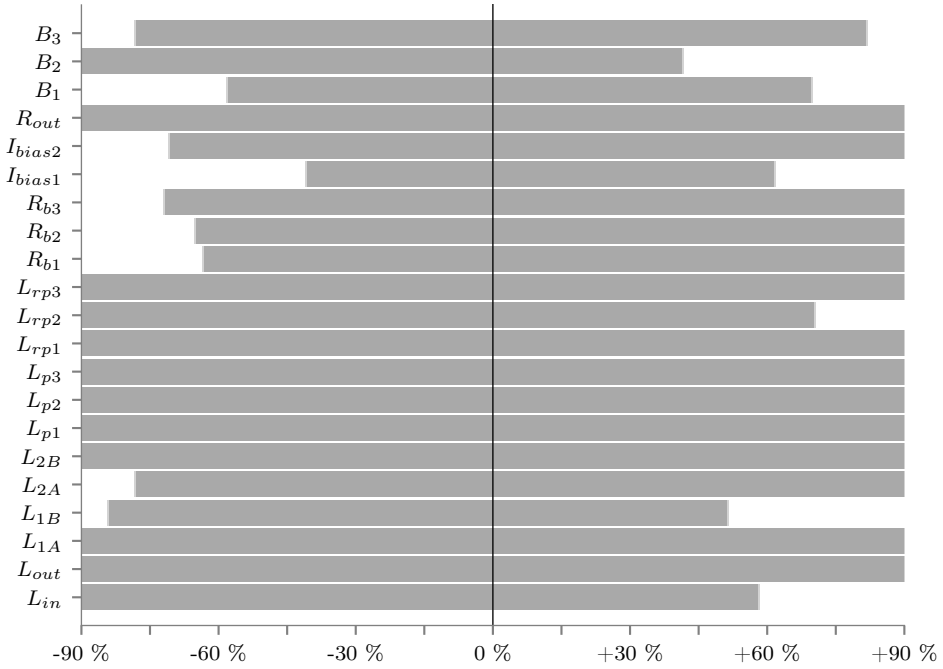

Figure 6.13: Basic optimized JTLT high speed margins

Design parameters	High speed optimized values
L_1	7.934 pH
L_2	7.972 pH
L_{in}	2.0 pH
L_{out}	2.0 pH
B_1	1.001 µm^2
B_2	1.023 µm^2
B_3	1.009 µm^2
β_1	3.929
β_2	1.013
β_3	3.375
χ_1	0.6422
χ_2	0.6285
χ_3	0.4613
R_{out}	1.3 Ω

Table 6.5: High-speed optimized JTLT design parameters

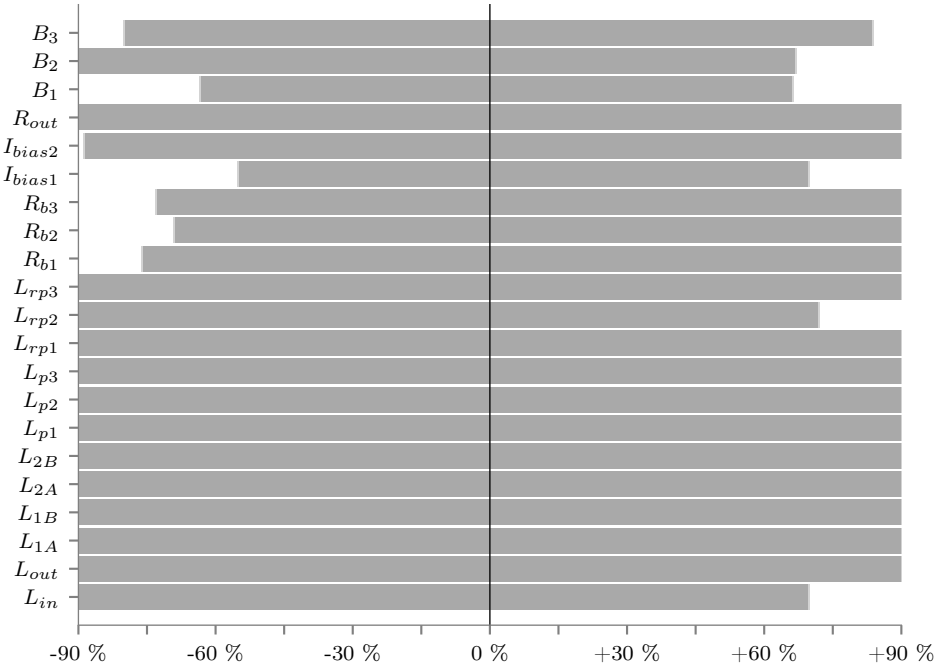

Figure 6.14: High speed optimized JTLT high speed margins

of the resonant JTLT structure with a test sequence is shown in Fig. 6.15.

We want to verify the JTLT structure when simulating it at resonance. It is computationally expensive to verify a wide range of frequency points using the resonance structure. To determine the best frequency point to verify the resonant operation, we sweep the frequency and calculate the margins in the global current directions. The margin vs frequency plot of the high-speed JTLT is shown in Fig. 6.16.

The upper failure corresponds to the JTLT being over-biased. This failure occurs at the same point in both the resonant and high-speed cases. In the lower failure margin, we can see peaks which correspond to some resonant frequency. The departure of the lower margin line from the high-speed failure lower margin in the non-resonant reason can be attributed to the attenuation of the pulse on the line.

The classical method to calculate resonance on a PTL does not correspond to a resonance peak. Two factors cause the classical method to fail. The first reason is that the primary source of weak noise is flux mismatch and not impedance mismatch. The flux is not reflected immediately upon arrival of the pulse, but is slightly delayed and is not reflected all at once. The second reason is that the PTL's wave velocity also varies with frequency, causing the noise to spread.

We note that the worst margin occurs at $\approx 94\,\text{GHz}$. This is slightly lower than our target operating frequency. To esnure that we optimize the JTLT for resonant without compromising the high speed performance we test the JTLT at 94 GHz as well as 100 GHz. The margins of the high-speed JTLT is shown in Fig. 6.17

Using the resonant verification procedure and the high speed optimized circuit as

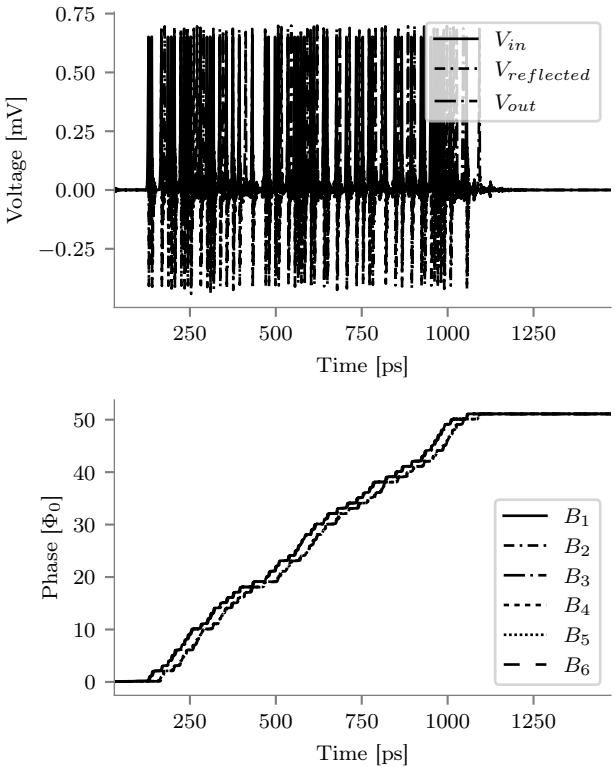

Figure 6.15: Resonant simulation of high speed JTLT

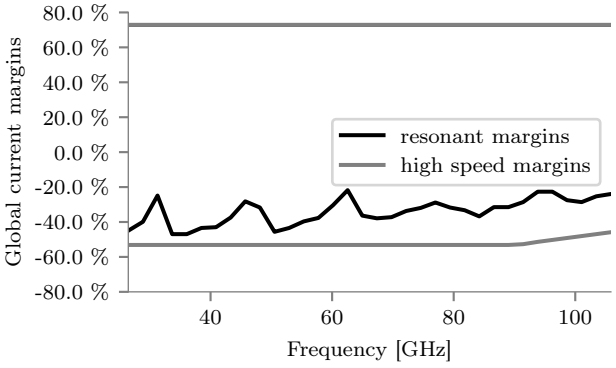

Figure 6.16: High speed optimized JTLT global current margins vs frequency

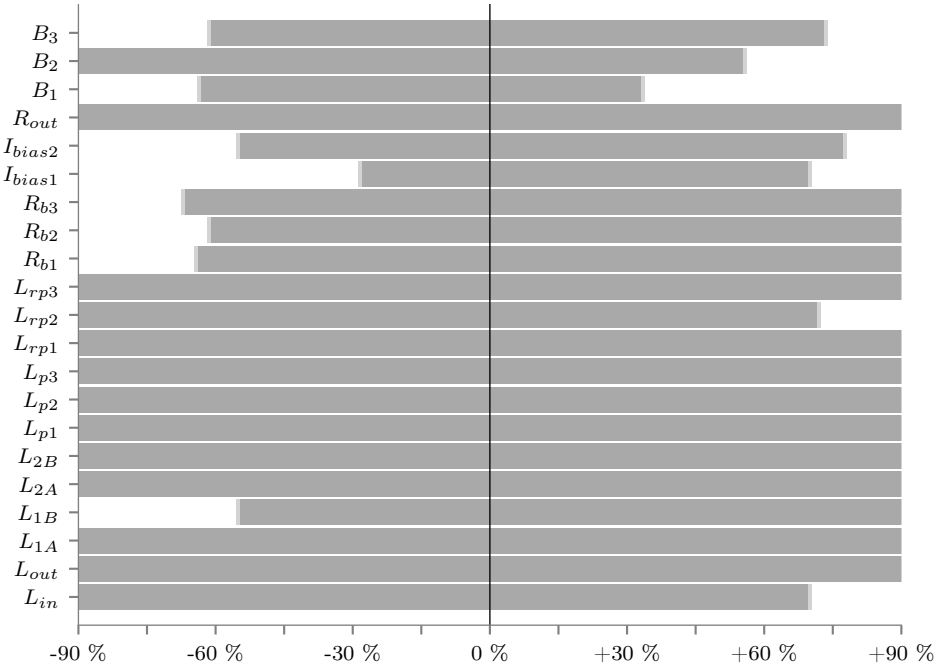

Figure 6.17: High speed optimized JTLT resonant margins

a starting point, we optimize the JTLT. The resonant optimized design parameters are shown in Table 6.6.

The margin analysis and the bias current margins over frequency is shown in Fig. 6.18, and Fig. 6.19, respectively.

The margins of the JTLT optimized for resonance is lower than the JTLT optimized for in simpler circuits. The reduction in margins is due to the resonance on the PTL. The circuit still operates at sufficient margins for reliable operation. The operating point seems to be, again, limited by the design boundaries.

6.7 Conclusion

In this chapter, we have gone over how all the methods that were developed in this thesis can be used to aid in the design of a simple SFQ circuit, the JTLT. Although the circuit is relative simple, complex dynamics complicate the design.

Design equations are essential for converting design parameters into circuit parameters. Without parasitic effects, such as in this case study, the design equation can be derived without the fundamental inductance model, but with little effort, parasitic effects can be included. The derivation is also straight forward requiring only undergraduate level engineering mathematics.

Currently, the complex high-frequency behaviour of an SFQ pulse on a PTL is only possible through numerical models. No analytical methods of analyzing how attenuated SFQ pulses interact with a receiving Josephson Junction currently exist.

Design parameters	Initial values
L_1	7.987 pH
L_2	7.551 pH
L_{in}	2.0 pH
L_{out}	2.0 pH
B_1	1.014 µm^2
B_2	1.011 µm^2
B_3	1.0 µm^2
β_1	3.98
β_2	1.278
β_3	3.904
χ_1	0.7037
χ_2	0.6809
χ_3	0.477
R_{out}	1.236 Ω

Table 6.6: Resonant optimized JTLT design parameters

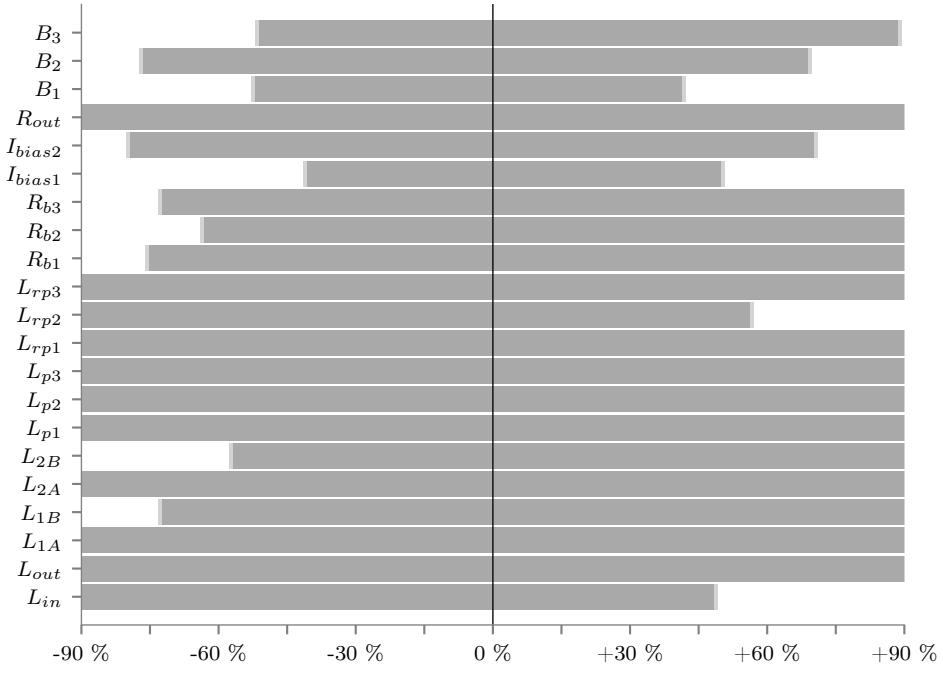

Figure 6.18: Resonant optimized JTLT resonant margins

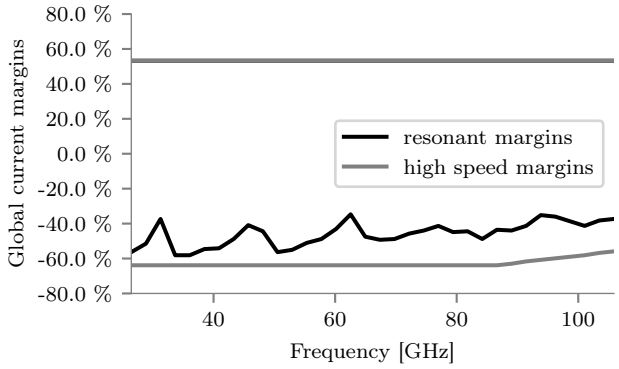

Figure 6.19: Resonant optimized JTLT global current margins vs frequency

Analysis including these effects requires numerical modelling of the phenomenon.

The necessity of numerical models imply the necessity of automated optimization tools. The developed DFM algorithm is capable of optimizing circuits with complex behaviour and producing significant improvements to suboptimal designs.

The choice of design boundaries limits the designed JTLT. Two main areas where the design can be improved are the verification function and the statistical process information. A noise-aware verification can add bit-error-rate requirements to the verification function allowing a more realistic working region of the circuit. Using statistical process variation information will allow yield optimization procedures to optimize the fabrication yield directly instead of optimizing other estimates.

Chapter 7

Conclusion

This dissertation discussed and developed methods necessary to improve high-frequency SFQ electronics design. The shortcomings of the previous methods range from poor performance to results that poorly correlate with the real world.

PTL lines are used as interconnects between cells and are an essential part of large scale SFQ digital electronics. PTLs exhibit complex high-frequency behaviour. We presented a 2D quasi-TM FEM solver that can efficiently solve the propagation properties of superconductor transmission lines. The solver is capable of handling the complex high-frequency material properties of superconductors.

The high-frequency response of superconductor structures need to be integrated into existing analysis frameworks. To this extent, superconductor vector fitting was developed to allow fitting high-frequency superconductor responses into a state-space model. The state-space model can be used directly or can be converted into an equivalent SPICE netlist. This allows engineers to take into account complex high-frequency effects that were not previously possible.

The dynamics of SFQ circuits are difficult to predict even before the introduction of high-frequency models. To ensure that circuits have the maximum probability of working when fabricated, they are designed for maximum fabrication yield. Automated yield optimization significantly improves designs and reduces engineering effort. A novel yield optimization method, DFM, was proposed that improved the quality of the optimized circuits over the current state of the art methods.

Inductance is one of the main components of superconductor circuits and yet is often poorly modelled. We propose the fundamental inductance model to model all inductive effects accurately. It also serves as a useful model during the design and analysis of superconductor circuits.

To show how these methods integrate into designing a simple SFQ cell, we demonstrated all these methods during the design of a simple JTLT. The fundamental inductance model was used to get the initial design equations. Time-domain models of high-frequency PTLs were used to simulate and verify the JTLT circuit. The newly developed optimization algorithm was used to centre the design at the optimal fabrication yield. The result was a robust JTLT circuit.

We have clearly shown that the methods developed improve the state of high-frequency SFQ design and adds useful and necessary tools to the toolbox of an SFQ

circuit designer. Many further opportunities for improvements are now exposed. The ultimate end-goal of engineering SFQ digital circuits to supersede existing technologies is one step closer.

Appendix A

Journal Paper: Modeling of Superconducting Passive Transmission Lines

- P. le Roux, K. Jackman, J. A. Delport, and C. J. Fourie, "**Modeling of Superconducting Passive Transmission Lines**," IEEE Trans. Appl. Supercond., vol. 29, no. 5, pp. 1-5, Aug. 2019.

The majority of the contributions to this article are my own. The co-authors provided the reference 3D simulation data from TTH. IEEE Transactions on Applied Superconductivity hold the copyright for this article.

Modeling of superconducting passive transmission lines

Paul le Roux, *Student Member, IEEE*, Kyle Jackman, Johannes A. Delport, *Student Member, IEEE*, and Coenrad J. Fourie, *Senior Member, IEEE*

***Abstract*—Superconducting technologies are moving towards very-large-scale integration (VLSI) of circuits. Passive transmission lines (PTLs) are used to quickly and efficiently propagate single flux quantum (SFQ) pulses between separated logic elements of these VLSI circuits. PTLs are often insufficiently modeled to correspond to reality. Therefore, the PTL needs to be thoroughly studied to determine realistic propagation characteristics. A quasi-transverse magnetic (TM) formulation is used to study superconducting passive transmission lines. The ambient temperature and changes in penetration depth with frequency are taken into account when solving the electromagnetic fields of a PTL. Per-frequency transmission line parameters are extracted from the quasi-TM field solutions. The results show a very close correlation to TetraHenry, an existing 3D solver, at significantly reduced computational cost. The results also clearly show that PTL propagation characteristics are sensitivity to frequency and temperature.**

***Index Terms*—passive transmission line (PTL), superconducting integrated circuits, transmission-line model.**

I. Introduction

THE distance that single flux quantum (SFQ) pulses need to be transmitted continuously increases as more complicated designs increase chip area. One aim of the SuperTools program is to develop a working 64-bit RISC superconducting microprocessor [1], [2] with the MIT Lincoln Laboratory (MIT-LL) SFQ5ee [3] process. Very-large-scale integration (VLSI) requires automated place-and-route tools [4], and these tools could create long routes between connected components. Superconducting passive transmission lines (PTLs) are used to transmit SFQ pulses across these long distances [5]. Dispersion and attenuation on the PTL can lead to timing variations and even operational failure. It is, therefore, essential to have an accurate model of the PTL. This research will present a method to calculate the propagation characteristics of long superconducting structures, such as PTLs, over a wide range of frequencies. The breakdown of superconductivity at high frequencies and the change in penetration depth due to the ambient temperature will be taken into account when solving the propagation characteristics.

Tremendous effort has gone into characterizing and optimizing PTLs along with the corresponding drivers and receivers [6]–[10]. Modeling a PTL as an ideal lossless transmission line ignores AC-losses in the superconductors. Linearizing the superconductivity effect at the point where the SFQ pulse carries maximum energy is more accurate, but it then incorrectly includes DC losses. Flux trapping cannot happen in a loop with DC losses, and this fundamental phenomenon is, therefore, not included in the model. Regardless of the technique used to model superconductivity, the transmission line parameters need to be calculated. The propagation characteristics of a specific line can be calculated with field solvers such as SONNET [7] and TetraHenry [11]. Analytical approaches to inductance extraction of superconducting lines also exist [12]. Unfortunately, 3D solvers are computationally expensive and analytical solutions are restricted to specific geometries.

The research is based upon work supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via the U.S. Army Research Office grant W911NF-17-1-0120, and based on the research supported in part by the National Research Foundation of South Africa (Grant Number: 105859). The authors are with Stellenbosch University, Stellenbosch, South Africa (e-mail:17500966@sun.ac.za)

II. Complex conductivity of superconductors

Superconductivity is a complex macroscopic quantum effect which is difficult to simulate fully. Many approximations can be made to make simulations of superconductors more practical. Approximating superconductivity with a complex conductivity expression, which accounts for the penetration depth, is the most widely used method when modeling superconducting circuits [13]–[16]. The complex conductivity can be substituted into Maxwell's equation to determine field solutions of superconductors. The complex conductivity approximation does not take into account the proximity effect on the superconductor boundaries [17] or the breakdown of superconductivity due to high applied currents or magnetic field [17]. Furthermore, in this study, the local temperature variation that arises from Joule heating is also ignored.

Zimmermann provides the most accurate complex conductivity expression for isotropic Type 2 superconductors [16], as far as we are aware. It takes into account the scattering time of electrons, and the expression is in terms of the material properties and temperature. If the superconductor is Type 1, the complex conductivity derived by Mattis [15] would be best suited. For anisotropic superconductors, a complex conductivity tensor would need to be used instead. The SFQ5ee process uses niobium, an isotropic Type 2 superconductor, and, therefore, this study will use Zimmermann's complex conductivity.

Zimmermann provides a software program that calculates the complex conductivity, but it uses an approximate expression for the gap energy and uses a limited integration routine. With advances in modern computing, it is no longer needed

to use an approximated expression, and the self-consistent gap energy integral equation [18], [19] was used to calculate the gap energy.

There is no closed form solution to the integral expression that describes the complex conductivity. Therefore, a numerical integration routine is required to evaluate the expression. The singularity in both I_1 and I_3, from Zimmermann's complex conductivity expression, corresponds to the weight function of the Gauss-Chebyshev quadrature. An adaptive Gauss-Chebyshev quadrature routine was used to integrate I_1 and I_3. I_2 was transformed using the same transform Zimmermann used and integrated with an existing adaptive quadrature routine [20]. Zimmermann's expression, in its original form, has a numerical instability in the clean limit where the scattering time, τ, goes to zero. This is the cause of the non-smooth surface resistance, calculated from Zimmermann's expression, noticed by Linden [14]. Multiplying τ into the integrands and simplifying leads to an expression which has no such numerical instability. This instability research increased the accuracy and reduced the time taken to calculate the complex conductivity expression.

III. Field solution of a transmission line

Superconducting transmission lines are becoming narrower and thinner, and as a result, the penetration depth has become significant relative to the thickness of the line. An accurate model of superconducting transmission lines, therefore, needs to take into account the changes in penetration depth with frequency. The quasi-transverse electromagnetic (TEM) formulation is, therefore, unsuitable. This research proceeds by using the quasi-transverse magnetic (TM) formulation [21] instead. The quasi-TM formulation assumes that the wavelength of the frequency is significantly shorter than the width of the line [21]. A wide PTL from literature is 20 μm [7]. A frequency of 15 THz has a wavelength of 20 μm. 15 THz is well beyond the $\sim$ 750 GHz at which niobium loses superconductivity. The quasi-TM approximation is, therefore, valid.

Plaza [21] uses an implied field dependence of $e^{-j\gamma z+j\omega t}$, where j is the imaginary unit, ω is the frequency in radians per second, γ is the propagation constant, z is the longitudinal direction, t is time, and e is Euler's constant. This research uses a field dependence of $e^{-\gamma z+j\omega t}$ instead. Equations from Plaza [21] are adapted to the implied field dependence of this research. The scalar electric potential equation, adapted from Plaza [21], is

$$\nabla_t^2 \phi = 0, \tag{1}$$

where ϕ is the electric scalar potential, and ∇_t is the tangential del operator.

The scalar electric potential is constant across conducting faces [21]. The center conductor is excited with a 1 V source by setting $\phi = 1$ across it. The remaining conducting faces are grounded by setting $\phi = 0$ across them. If there are multiple dielectrics, then the change in the normal derivative of ϕ needs to be enforced.

There are three equations, listed by Plaza [21], that could be used to solve the remaining fields. Plaza [21] chose to solve the current equation using a method of moments (MoM) formulation. The mesh size that is needed to model the penetration depth accurately makes the MoM formulation impractical. Instead, the scaled longitudinal component of the magnetic vector potential, $\frac{A_z}{\gamma}$, will be solved with the finite element method (FEM). The equation, adapted from Plaza [21], is

$$\nabla_t^2 \frac{A_z}{\gamma} - j\omega\mu_0\sigma\frac{A_z}{\gamma} = -\mu_0\sigma\phi, \tag{2}$$

where μ_0 is the permeability of free space, and σ is the conductance of the material. If both ϕ and $\frac{A_z}{\gamma}$ are known, then the transmission line parameters can be determined [21].

To solve equation (1) and (2) with FEM, they need to be transformed into their equivalent weak formulation. Equation (1) in weak form is

$$-\iint_\Omega \nabla_t w \cdot \nabla_t \phi \; dx + \oint_{\partial\Omega} w \nabla_t \phi \cdot \hat{n} \; ds = 0, \tag{3}$$

where w is the testing function, $\hat{n}$ is the outward normal of the boundary, Ω is the domain, $\partial\Omega$ is the boundary of the domain, dx is the surface differential, and ds is the boundary differential. Equation (2) in weak form is

$$\begin{aligned} -\iint_\Omega \nabla_t w \cdot \nabla_t \frac{A_z}{\gamma} \; dx + \oint_{\partial\Omega} w \nabla_t \frac{A_z}{\gamma} \; ds \\ -j\omega\mu_0 \iint_\Omega \sigma w \frac{A_z}{\gamma} \; dx = -\mu_0 \iint_\Omega \sigma w \phi \; dx. \end{aligned} \tag{4}$$

Both problems have an open boundary, but for convenience, a perfect electric conducting (PEC) boundary was used. The PEC boundary was shifted away from the PTL until it made a negligible difference in the field surrounding the PTL. On the PEC boundary, $\phi = 0$ and $A_z = 0$. This Dirichlet boundary condition implies both the testing functions are zero on the boundary. The contour integrals, therefore, are then both zero.

FEniCS [22], a FEM library, was used to solve (3) and (4). FEniCS does not yet support complex numbers directly. The matrices and vectors were, therefore, computed with FEniCS, exported to NumPy arrays [23], multiplied by the complex coefficients, and then solved.

IV. Transmission line model

The model described by the telegrapher equations, as shown in Fig. 1, uses a complex inductance, $\hat{L}$, and capacitance, $\hat{C}$, to include losses [21]. The inductance and capacitance per unit length were calculated per frequency to model the frequency dependent characteristics of the PTL accurately.

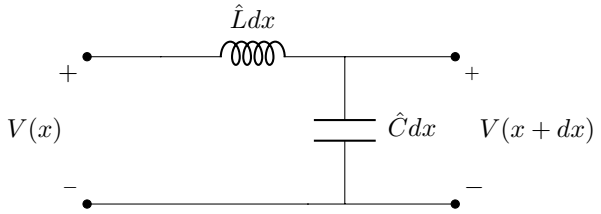

Fig. 1. Circuit diagram of telegram model adapted from [21]

The equations required to extract the transmission line parameters, adapted from Plaza [21], are

$$\hat{C} = -\oint_{\partial\Omega_e} \epsilon \nabla_t \phi \cdot \hat{\mathbf{n}}\, ds, \tag{5}$$

$$\frac{I_z}{\gamma} = -j\omega\sigma\frac{A_z}{\gamma} + \sigma\phi, \tag{6}$$

$$\frac{I}{\gamma} = \int_{\Omega_e} \frac{I_z}{\gamma} dx, \text{ and} \tag{7}$$

$$\hat{L} = \frac{1}{\omega\frac{I}{\gamma}}, \tag{8}$$

where Ω_e is the excited conductor face in the cross-section, $\partial\Omega_e$ is the boundary of the excited conductor face, ϵ is the permittivity, I_z is the current density, and I is the current through the excited inductor.

V. Comparison and Results

The results and comparisons are done with a 4.5 μm PTL [8] designed for the MIT-LL SFQ5ee process.

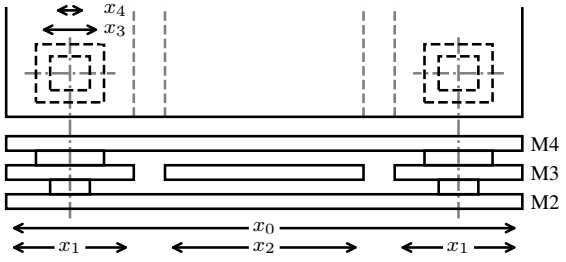

Fig. 2. PTL illustration with the accentuated features for visibility

Fig. 2 shows an illustration of the PTL. All layers have a thickness of 200 nm, and $x_0 = 9.1$ μm, $x_1 = 1.8$ μm, $x_2 = 4.5$ μm, $x_3 = 1.2$ μm, and $x_4 = 0.6$ μm The ground-plane and sky-plane, of the MIT-LL PTL, are continuously stitched with a stitch pitch of 5 μm. The 2D FEM formulation ignores such 3D effects. The PTL was simulated using TetraHenry with a coarse mesh, a fine mesh, with stitching, without stitching, and compared to the new 2D FEM solver. The initial comparison was made using the two-fluid model (TFM) conductivity with a typical penetration depth of 90 nm. Data on the dielectric losses over frequency in the SFQ5ee process were unavailable, so a lossless dielectric with $\epsilon = 4.6\epsilon_0$, where ϵ_0 is the permittivity of free space, was used.

TABLE I
Comparison with different engines, meshing, and stitching using the TFM

Engine	Stitching	Meshing	Capacitance	Inductance
TH	No	Coarse	-	54.56 nH $\cdot$ m^{-1}
TH	Yes	Coarse	-	54.54 nH $\cdot$ m^{-1}
TH	No	Fine	2.013 nF $\cdot$ m^{-1}	53.17 nH $\cdot$ m^{-1}
TH	Yes	Fine	2.014 nF $\cdot$ m^{-1}	53.17 nH $\cdot$ m^{-1}
FEM	No	Fine	1.952 nF $\cdot$ m^{-1}	53.32 nH $\cdot$ m^{-1}

Table I tabulates the results. The capacitance is quick to calculate with TetraHenry, even with the fine mesh, so only the fine mesh was used for comparison. The difference in capacitance is because TetraHenry takes into account additional fringe fields from the ports. These fringe fields are not present in an actual PTL. The per-unit inductance of TetraHenry using the finer mesh closely matches the 2D FEM formulation where the coarse mesh slightly over-estimates the inductance value. The stitching has a negligible effect on the extracted parameters, and can, therefore, be ignored.

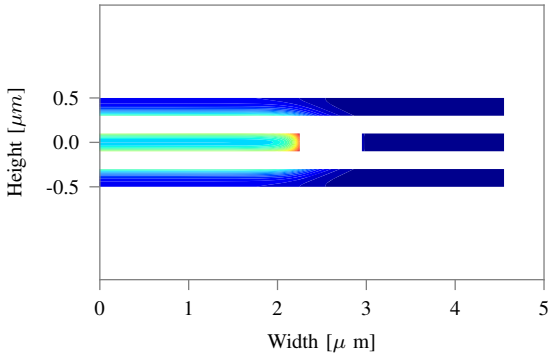

Fig. 3. Scaled current density, $\frac{I_z}{\gamma}$, of the PTL under study with the TFM

Fig. 3 shows the scaled current density of the MIT-LL PTL. On inspection, Fig. 3 shows a high current density on the corners of the PTL. Applying a sufficiently large excitation to the PTL will, therefore, cause superconductivity to start breaking in the corners of the center conductor and cause the surrounding area to heat up. This method of analysis is, therefore, only valid when the breakdown of superconductivity, in the corners, is negligible.

Zimmermann's complex conductivity expression was used to do a frequency sweep of the MIT-LL PTL at 4 K with TetraHenry and the to determine the per-unit inductance and resistance. The material parameters of niobium were obtained from Pronin [24].

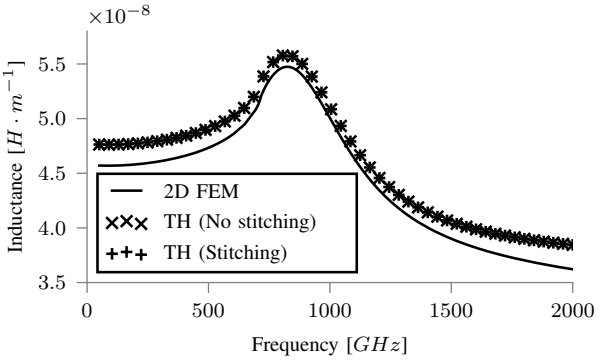

Fig. 4. The frequency dependant inductance per meter of the PTL under study at 4K

Fig. 4 and Fig. 5 shows the per-unit inductance and resistance extracted with the new 2D FEM formulation and TetraHenry. TetraHenry was run with the coarse mesh and as

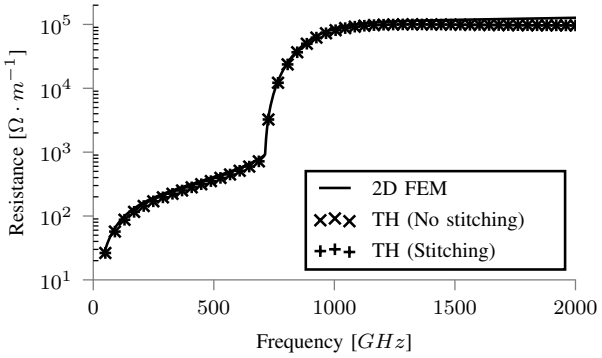

Fig. 5. The frequency dependant per unit length resistance of the PTL under study at 4K

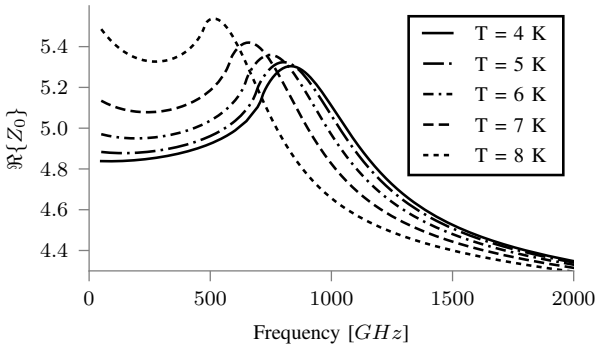

Fig. 8. The frequency dependant real component of the characteristic impedance of the PTL under study

expected has a slightly higher inductance value. The results match closely even at high frequencies. TetraHenry can be used to extract the transmission line parameters, but it's significantly slower than the specialized 2D FEM solver. The faster solver makes it possible to do frequency sweeps at varying temperatures quickly.

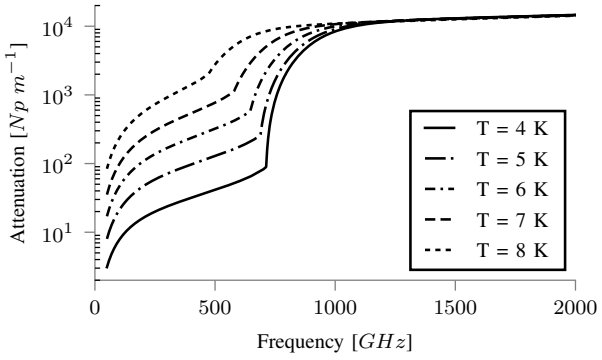

Fig. 6. The frequency dependant attenuation of the PTL under study

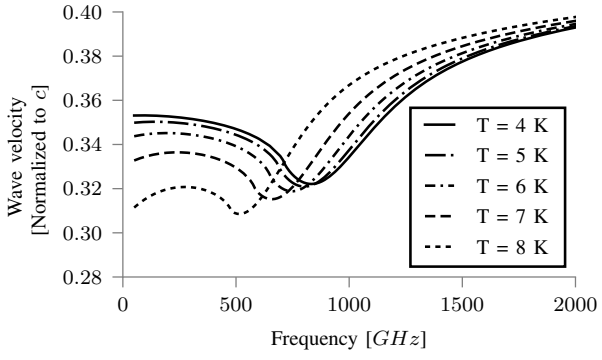

Fig. 7. The frequency dependant wave velocity of the PTL under study

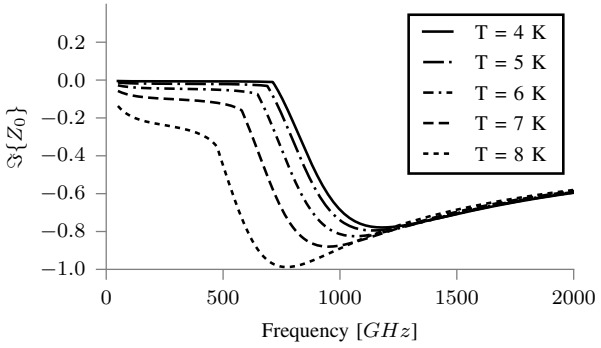

Fig. 9. The frequency dependant imaginary component of the characteristic impedance of the PTL under study

Fig. 6, 7, 8, and 9 shows the characteristics of the lines over frequency at varying temperatures. The response is not consistent across frequency and varies significantly with changes in ambient temperature.

VI. Conclusion

The numerical method to calculate complex conductance expression from Zimmermann [16] was improved. A technique that can be used to determine the propagation characteristics in arbitrary superconducting structures was shown. The technique matches much slower 3D methods and is accurate for a wideband frequency range. This wideband frequency model will be used in future work to derive a SPICE model of the PTL. The SPICE model will then be implemented into JoSIM [25] to investigate what effect a PTL has on superconducting logic circuits.

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Appendix B

Journal Paper: Distance-to-Failure-Maximization optimization algorithm for SFQ logic cells

- P. le Roux and C. J. Fourie, "**Distance-to-Failure-Maximization optimization algorithm for SFQ logic cells**," IEEE Trans. Appl. Supercond., vol. 30, no. 7, pp. 1-5, Oct. 2020.

Distance-to-Failure-Maximization optimization algorithm for SFQ logic cells

Paul le Roux, *Student Member, IEEE*,
and Coenrad J. Fourie, *Senior Member, IEEE*

***Abstract*—SFQ logic (such as RSFQ and ERSFQ) is one of the contenders for future low power, high-speed electronics. SFQ logic can also function as the interface to superconducting quantum qubits. It is therefore essential to have robust SFQ cells libraries that can be used in these designs. One significant challenge in SFQ circuit design is to find the best-optimized design, starting from a nominal working circuit, that circuit designers should layout. Various optimization algorithms and tools are available (such as Largest Inscribed Hypersphere, Critical Margin optimization, Particle Swarm, and various other algorithms), but all of them have different shortcomings that make it difficult to use with real-world cells. We present a new optimization algorithm, the Distance-to-Failure-Maximization (DFM) method, that uses some of the insight of the previous algorithms as well as a few new characteristics that make the optimization algorithm practical to use in real-world cases. We also provide an open source implementation that was used to optimize real-world RSFQ cells for the ColdFlux project. We compare the optimization algorithm with other approaches and show the improvements above the current state of the art.**

***Index Terms*—Circuit optimization, RSFQ logic.**

I. Introduction

SUPERCONDUCTOR integrated circuits are becoming larger and more complex in an effort to scale these to challenge existing technologies. These Very Large Scale Integration (VLSI) circuits require robust circuit cells with very high yield.

Numerous optimization methods exist, such as Inscribed Hyperspheres [1], Center of Gravity Method (CGM) [2]–[4], Single parameter optimizations and variations thereof [5]–[7].

MALT is an older optimizer that searches for the largest inscribed hypersphere in the valid region approximated by a convex hull [1]. It is computationally expensive and makes an error by optimizing for the largest working hypersphere without accounting for percentage scaling of parameters. The valid region is also not perfectly convex [1]. There are transforms that can be applied to make the valid region approximately convex in some cases [1], but an error is still incurred.

The ‘xopt‘ utility uses CGM to optimize a circuit [3], which can fall within a non-working region (even if cluster analysis can warn against the possibility of such results). It scales poorly with higher parameter counts.

COWBoy, the optimizer included in PSCAN and PSCAN2, does a sequence of single parameter optimizations [5], [6], [8]. This technique, although simple, is remarkably effective in quickly improving margins. The method sometimes optimizes to non-optimal points since it locks into a region where changing any single parameter results in a worse circuit.

Cadence AAO has made significant progress in SFQ circuit optimization and has shown a method to localize which components are close to the point of failure [7]. Random sampling works well for a small number of components, but becomes expensive at higher dimensions.

Stochastic optimization methods, such as genetic algorithms [9] and particle swarm [10], have also been shown to work well when optimizing circuits. These optimization methods, when left to completion, perform well, but require a large number of score evaluations to complete. A large number of score evaluations can quickly become computationally costly. These methods parallelize well and are viable options if computational power is not restricted.

II. Circuit score

An optimizer maximizes some score function. In practice, multiple metrics are looked at when judging the feasibility of a circuit, but an optimizer needs a function which reduces to a single value. Different metrics of scoring circuits include yield analysis, yield roll off analysis, critical margin, etc.

Yield and yield roll-off are the best circuit metrics to use, but are expensive to compute and do not give stable results due to their stochastic nature. An optimizer can, therefore, not use yield or yield roll-off as a score function.

Critical margin analysis is the most used score amongst different optimization methods [5]–[7], [9]. Although there are drawbacks, it is an excellent metric for scoring a system quickly. It is done by doing a margin analysis and taking the worst margin as the critical margin. The margins are usually calculated with a binary search scheme for computational efficiency. In some cases, there can be dead zones in the margins which the binary search can miss. This can be alleviated by first scanning the line with a fixed step size using a binary search only to refine the closest point of failure, but this is seldom done in practice. This will cause some margin to be artificially high. Margins also only look at a small area of the parameter space. In higher dimensions, the space is too large to search extensively, and this is an acceptable compromise.

There is, however, room for improvement. During optimization, many margin analyses are done, and many points of failure on the valid region’s boundary are computed. Instead of doing only a margin analysis, we look for the statistically nearest point

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of failure using the Mahalanobis distance. The Mahalanobis distance, D_M, is defined as

$$D_M(\mathbf{x}, \boldsymbol{\mu}, \mathbf{S}) = \sqrt{(\mathbf{x} - \boldsymbol{\mu})^T \mathbf{S}^{-1} (\mathbf{x} - \boldsymbol{\mu})} \quad (1)$$

where $\mathbf{x}$ is the coordinate, $\boldsymbol{\mu}$ and $\mathbf{S}$ is the mean and covariance matrix of the distribution, respectively [11].

The score function, f, is then defined as

$$f(\mathbf{x}) = \min(\{D_M(\mathbf{x}_f, \mathbf{x}, \mathbf{S}(\mathbf{x})) \mid \mathbf{x}_f \in H_f\}) \quad (2)$$

where H_f is a set of all the known points of failure and S is a function dependant on x which defines the covariance matrix. The function, S, is dependant on the specific design and is considered prior knowledge.

If we only have a single margin analysis, the closest point of failure is the critical margin. This also makes changing the parameter distribution as easy as changing the distribution used to calculate the Mahalanobis distance. This score function tends to move away from points of failure in contrast to the CGM, which moves towards points of success.

III. Optimization Method

The DFM method repeatedly tries to guess the point in the parameter space which is furthest away from all known-points-of-failure. Each guess is analyzed to improved the knowledge about the parameter space for subsequent guesses. This is repeated until convergence or the maximum number iteration has been reached. Fig. III shows the algorithm flow. The explanation of each step follows:

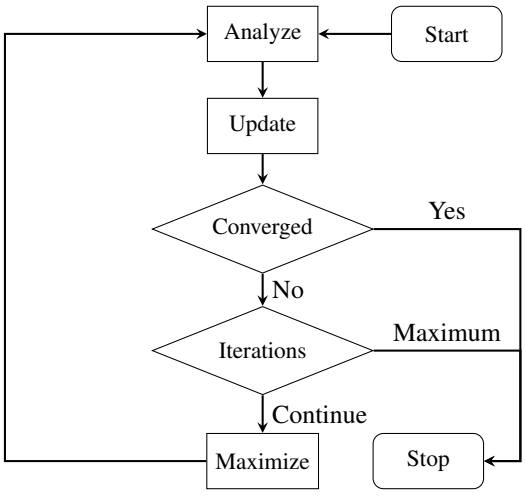

Fig. 1. Optimizer flow graph

1) **Start**: Set the initial best guess to the parameters of a working circuit. Set the guessed best score to infinity.
2) **Analyze**: Analyze the guessed best point. The analysis involves doing line searches in various directions in the parameter space to determine failure points on the boundary of the valid region. In our implementation, a margin analysis is used, but a different set of directions can be chosen that corresponds to the most likely failures of the cell.
3) **Update**: Given the new points of failure, update the actual score for all previous guesses. Set the new current best point to the point with the best actual score.
4) **Converge**: If the actual score of the current guess is sufficiently close to the actual score of the guessed point, then convergence was reached and optimization terminates.
5) **Maximum iteration reached**: If the maximum number of iterations is reached, then terminate the simulation. Otherwise, continue to the maximize step.
6) **Maximize**: The region around the current best guess is searched for a point which is statistically the furthest away from all known points of failure. This is done using a differential evolution (DE) algorithm [12]. The new best guess is checked to ensure that it is valid before continuing to the analyze step. If it is not valid, then add the point to the known-points-of-failure and the maximize step is restarted.
7) **End**: Save the current best point as the optimized output.

All guessed points are taken into consideration in step 3. This is necessary since new points of failure could have been discovered which worsen the scores of previous guesses. This addresses a subtle shortcoming of most other optimization techniques that only use a single margin analysis as a score function. If the scores of the previous guesses are not updated, the optimization process might converge to an artificially high score function induced by either missed margins or close points of failure not found by the margin analysis.

Our implementation is open-source and freely available [13]. The optimizer was used during the design of the Stellenbosch RSFQ cell library [14]. We believe that these real-world results show that the DFM algorithm scales and is usable on practical circuits The current version of JoSIM Tools, at the time of writing, is v1.0.2. This tool was developed with a focus on SFQ circuits, but the DFM algorithm is general and not limited to SFQ.

We used the DE algorithm implementation from scipy [12], [15]. A population size of 25 times the number of parameters was used, and the recombination and mutation constants were left on their defaults. We found these parameters worked well.

IV. Performance Analysis

The optimization method is stochastic and is subject to variation both in the runtime and final score of an optimization run. The new optimization method was run on the RSFQ DFF analyzed in [7]. The optimization was run 100 times from the same starting point. The results were processed and analyzed.

All the optimization runs terminated with a point of failure closer than what any of the margin analysis predicted. This mode of termination highlights the importance of not only looking at the margin analysis. If a better line search were chosen so that a point closer to the actual closest point of failure was found, then the optimization will be able to continue and improve the optimization result further. Choosing the basis line searches is dependent on the cell being optimized and is outside the scope of this paper.

Fig. 2 shows comparisons of the time taken to optimize the cell and the resulting optimized cell's score. From Fig. 2 it is

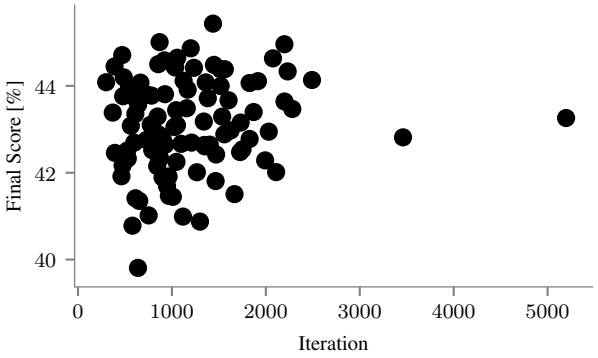

Fig. 2. Comparison of time taken by simulation and resulting optimized cell

clear that there is no correlation between the runtime of the algorithm and the final optimized cell. The temporal variation comes from the differential evolution step and the direction of the next best guess. The differential evolution step does not have a fixed runtime due to the stochastic nature of the algorithm. The next best guess can be in the correct direction, or it can first repeatedly guess in the wrong direction leading to additional iterations. The optimized difference comes from the simulations terminating due to there being a closer point of failure than the margin analysis predicts.

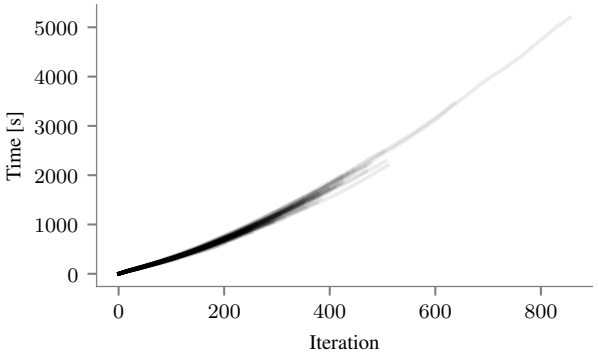

Fig. 3. The cumalitive time taken per iteration

Fig.3 shows the cumulative time taken per iteration for all the runs. A slight increase in time per iteration can be seen as the iteration number increases. This is because more known points of failure need to be taken into account. This increase is inevitable but might be reduced by filtering points that cannot be the worst point of failure. Fortunately, this increase is small, and the optimization times remain reasonable.

Fig. 4 shows the current best score per iterations for all the runs. For this cell, the score increases quickly at first, but then slowly increases until termination. The current best score can decrease per iteration as more points of failure become known. We, therefore, recommend that the simulation is not terminated as the score increase starts to plateau as the current best score is possibly over-estimated in the early stages of the algorithm.

Fig. 5 shows the mean time breakdown of the different parts of the optimization. The analysis step takes a relatively consistent amount of time during the optimization procedure.

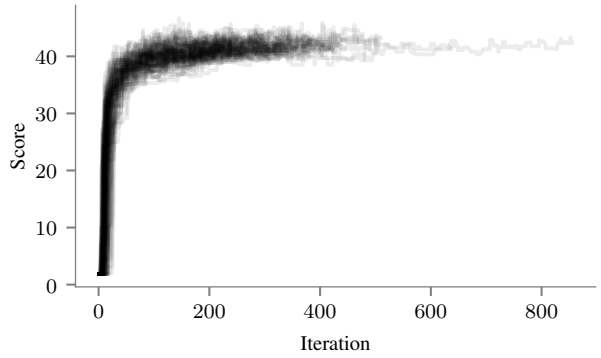

Fig. 4. The score plotted as the optimization progresses

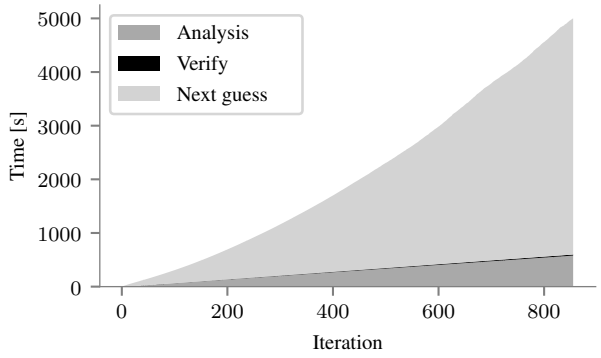

Fig. 5. The cumalitive time breakdown of iterations

The verification of guessed points takes an almost negligible amount of time. The time taken by determining the next guess is dominant. Any improvements in optimization speed should focus on improving the performance of determining the next guess and reducing the number of iterations required.

V. Comparison

We outline the differences in some of the different scoring types by doing a abstract comparison in two dimensions of an SFQ circuit's total current and total junction valid region. We used an RSFQ splitter cell with integrated transmission line drivers and receivers developed for the ColdFlux project [14], [16]. Two parameters, $Itotal$, and $Btotal$, are used as a coordinate system. These parameters are multiplied with each of the nominal current values and nominal junction areas to get the current values and junction areas of the circuit under test, respectively. We adaptively sample radially outward from a single point, $(1, 1)$, until a valid region boundary is constructed with sufficient accuracy. We then determine optimal critical margins, maximum distance to a point of failure and the largest hypersphere inscribed in the region's convex hull. Each of the previous point's critical margin, nearest failure and yield analysis score was calculated. The yield analysis score was calculated with 1,000,000 samples from a normal distribution centered on the point with a standard deviation of 0.15 scaled by the points position in the parameter space.

TABLE I
DFF OPTIMIZATION MARGIN COMPARISONS

Parameter	Starting Values			Cadence AAO			JoSIM Tools		
	Value	*Lower Margin*	*Upper Margin*	*Value*	*Lower Margin*	*Upper Margin*	*Value*	*Lower Margin*	*Upper Margin*
Itotal	-	3.0 %	41.8 %	-	> 90 %	86.8 %	-	84.4 %	70.1 %
Jtotal	-	13.1 %	2.4 %	-	38.9 %	> 90 %	-	46.3 %	75.4 %
Ltotal	-	14.7 %	5.3 %	-	40.0 %	69.8 %	-	52.3 %	62.3 %
Rtotal	-	19.0 %	> 90 %	-	85.7 %	90.0 %	-	84.7 %	> 90 %
LD	5.136 pH	> 90 %	3.5 %	2.037 pH	> 90 %	> 90 %	2.278 pH	> 90 %	> 90 %
LQ	3.945 pH	4.3 %	43.2 %	6.39 pH	36.5 %	64.5 %	6.180 pH	42.6 %	66.1 %
LO	4.34 pH	> 90 %	> 90 %	4.34 pH	78.6 %	> 90 %	3.895 pH	89.0 %	90.0 %
LREL	3.82 pH	> 90 %	19.9 %	2.092 pH	> 90 %	> 90 %	2.105 pH	> 90 %	90.0 %
J1	257.5 μA	6.8 %	4.4 %	239.2 μA	46.0 %	50.4 %	260.2 μA	45.7 %	44.5 %
J2	245 μA	12.4 %	1.9 %	176.6 μA	40.9 %	65.9 %	223.9 μA	47.6 %	55.3 %
J3	243.75 μA	72.8 %	12.6 %	223.4 μA	36.8 %	51.0 %	227.9 μA	43.0 %	47.6 %
J4	262 μA	11.2 %	19.0 %	247.9 μA	60.7 %	37.2 %	240.8 μA	61.3 %	45.7 %
I1	150 μA	3.0 %	41.8 %	144.9 μA	> 90 %	86.8 %	1.827 μA	84.4 %	70.1 %

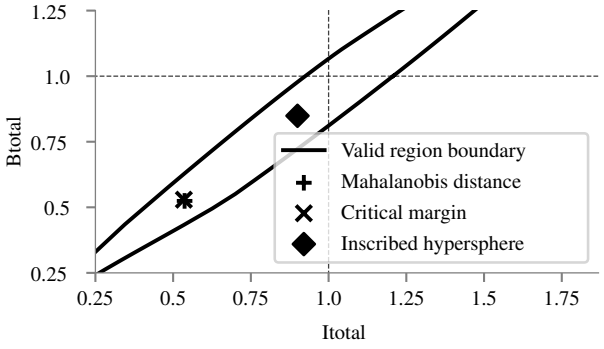

Fig. 6. Different score function visualization

TABLE II
DIFFERENT SCORE FUNCTION COMPARISON

Score function optimized	Comparison		
	Critical Margin	*Nearest failure*	*Yield analysis*
Critical Margin	18.2 %	13.0 %	64.4 %
Nearest failure	17.2 %	14.1 %	64.6 %
Inscribed Hypersphere	13.6 %	9.5 %	48.6 %

TABLE III
DFF OPTIMIZATION COMPARISON SUMMARY

	Starting Values	Cadence AAO	JoSIM Tools
Critical Margin	1.9 %	36.5 %	42.6 %
Critical Paramter	J2	LQ	LQ
Yield	6.6 %	50.2 %	52.8 %

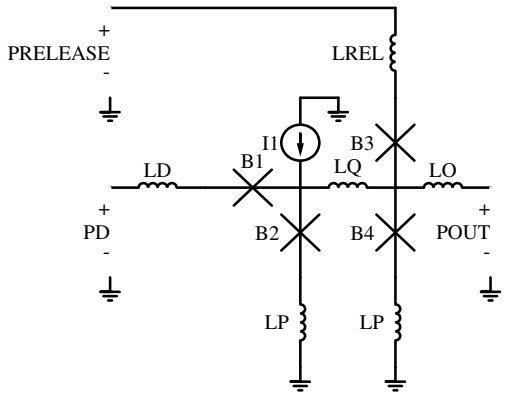

Fig. 7. Cadence DFF Example (Reproduced from [7])

Table II and Fig. 6 shows the comparison between the different optimization score functions. The inscribed hypersphere method is descent, but it is far from optimal. The critical margin method is a very good estimate of how a circuit works and the optimal critical margin is close to the actual optimal point, and there is room for improvement. The nearest failure maximization gives the best result here.

The new optimization method was compared to Cadence AAO on the DFF that was optimized in [7]. Fig. 7 shows the DFF. Table I and III tabulates the results. The upper margin and lower margin refer to the amount a parameter can be increased and decreased, respectively, before the circuit stop working. The differences in calculated margins are a result of differences in the testbench setup. Cadence AAO was not available so that we used optimized values directly from [7]. The COWBoy optimized values, as reported by [7], fails validation when the the D-input is pulsed twice and we did not include it in our comparison. The yield analysis was performed with a normal distribution with μ equal to the nominal value and $\sigma = 0.2\mu$ for all parameters. The results show that our optimization method performs better on a real world cell, the DFF, than Cadence AAO. Both the critical margin and yield was improved resulting in a more robust cell.

VI. CONCLUSION

We presented a new optimization algorithm, the DFM method, that maximizes the closest distance to failure. This method improves on the current state of the art critical margin optimization. We shown that the DFM method outperforms existing tools such as Cadence AAO. This method is extendable with the insights behind Cadence AAO localized optimization and global verification. This would allow optimizing large circuits effectively and would be the focus of future work on JoSIM Tools.

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Appendix C

Journal Paper: Fundamental Inductance Modelling and its implications in superconductor circuit design

- P. le Roux, L. Schindler, and C. J. Fourie, "**Fundamental Inductance Modelling and its implications in superconductor circuit design**," IEEE Trans. Appl. Supercond.

The majority of the contributions to this article are my own. The co-authors provided the design equation foundations on which the fundamental loop design equations were based. If the publication is accepted for submission, the copyright will be transferred to IEEE Transactions on Applied Superconductivity.

Fundamental Inductance Modeling and its implications in superconductor circuit design

Paul le Roux, Lieze Schindler, Coenrad Fourie, *Senior Member, IEEE*

***Abstract*—Superconductor circuits, such as AQFP and RSFQ logic cells, are sensitive to inductances. Most circuit models partially or completely ignore parasitic mutual inductances leading to circuits that appear to work in simulation but fail in practice where mutual coupling can have significant effects. We show a method to model purely inductive networks that can be used to accurately take mutual coupling into account. We apply this fundamental inductance model to a few different types of superconductor circuits to show the design implications. We present how the more accurate inductance model changes the potential energy of an AQFP gate. We demonstrate how to identify and design for potential parasitic coupling in a basic RSFQ PTL repeater. We also show that unaccounted parasitic coupling introduces significant error in parameter extraction in SQUID arrays. We conclude with the need to use the fundamental inductance model when designing circuits in a parasitic environment.**

***Index Terms*—Inductance, Superconducting integrated circuits, SQUIDs**

I. Introduction

SUPERCONDUCTOR circuits are becoming larger and more complex as superconductor circuits are improved and scaled to challenge existing technologies. The IARPA C3 project [1] provided development stimulus to scale up superconductor circuit complexity. Superconductor digital electronics can potentially offer improved power-efficiency, and increased performance over existing semiconductor technologies. Superconductor digital electronics also commonly operate at cryogenic temperatures and are naturally suited to interface with qubits [2]. The required number of wires per qubit within quantum computers need to be reduced to be able to scale enough to surpass existing solutions [3]. A superconductor processor could dramatically reduce the number of wires that are required to operate a quantum computer.

Superconductor analogue electronics also offer vastly superior sensor capabilities in certain areas, and are used for superconducting single-photon detectors, superconductor quantum interference devices (SQUIDs) for magnetometry, superconductor quantum interference filters (SQIFs), and superconductor gradiometers.

Inductances and Josephson junctions are the fundamental circuit elements in superconductor digital circuits. Accurate extraction and modeling of inductances are essential to the modeling and design of superconductor circuits. Any error in inductance extraction directly increases the error of the circuit model, where current distribution, switching dynamics and magnetic coupling are functions of inductance. This could lead to a circuit that works in simulation, but not when fabricated. Poorly modeled inductances are often the cause of circuit failure but are very seldom considered as the reason for failure. Other effects such as rogue flux trapping, bias current magnetic fields or local heating are often presented as the cause of circuit failure, but these are seldom validated.

Significant work has been done on ensuring reliable field solutions for the calculation of inductance in superconductor structures [4]–[6], but more attention is needed for the modeling of inductance networks to which to fit the results of field calculations. Through developing a method to extract inductances accurately and measuring the error that occurs in the extraction process, we significantly improve the engineerability of superconductor circuits.

A. Existing methodologies

Two main inductance extraction methodologies have been identified. In the absence of formal naming conventions for the methodologies, we will refer to them as local block-based extraction (per-square estimation [7]) and field-based extraction (determining a compact model from the solutions of Maxwell's equations).

Local block-based estimation tends to be quick and can scale to large circuits efficiently, but can potentially give inferior accuracy. One calculates the effective kinetic and self-inductance per unit area and then the inductance of a structure is calculated by looking at the area of the structure. This can be very accurate for long inductive structures with simple current return paths, but when considering more complex structures, the error can easily be large enough that the physical circuit fails. The error arises from inadequate estimation of inductance around corners, through vias, from neglecting all magnetic coupling and because current return paths are often estimated incorrectly.

Field based extraction tends to be slower, but can give very accurate results. One solves Maxwell's equations for the circuit and uses the current and voltages as seen from the ports to determine the inductances. If the circuit is accurately modeled by the field solver then the extracted inductances can be almost exact. The process is explained in [4]. In [4] the partial element equivalent circuit (PEEC) method is used to solve Maxwell's equation in magneto-quasistatic form, but any field solver can be used. A brief summary of how the process works is given below.

For accuracy, we will work on improving the field-based inductance extraction method as the local block-based method has intrinsic accuracy issues. There are hybrid approaches to

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inductance extraction that have been proposed. The approach solves the field in a local area and uses that to determine a more accurate inductance of the block. This addresses some of the shortcomings of the local block-based methods, but since magnetic inductance is a global effect, it is not taken into account by looking at local effects.

II. Inductance Models That Ignore Mutual Inductance

In cases where mutual inductances are negligible, they can safely be ignored. Unfortunately, the assumption is seldom checked. To analyze the error of ignoring mutual inductance we analyze two coupled inductor segments, shown in Fig. 1.

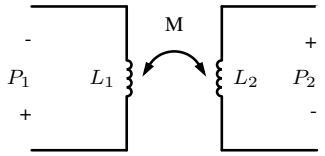

Fig. 1. Two inductors with mutual coupling.

Applying Kirchoff's Voltage Law on the two loops of the circuit gives us the following set of equations:

$$0 = V(P_1) - j\omega L_1 I_1 + j\omega M I_2 \tag{1}$$
$$0 = V(P_2) - j\omega L_2 I_2 + j\omega M I_1 \tag{2}$$

Given $V(P_1)$ and $V(P_2)$, we can solve I_1 and I_2 as:

$$I_1 = \frac{V(P_2)M + V(P_1)L_2}{j\omega(L_1L_2 - M^2)} \tag{3}$$
$$I_2 = \frac{V(P_1)M + V(P_2)L_1}{j\omega(L_1L_2 - M^2)} \tag{4}$$

To introduce an error term we attempt to model the results to the circuit, as shown in Fig. 2.

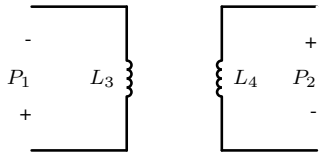

Fig. 2. Two inductors without mutual coupling.

Firstly, we investigate the rudimentary case where the a port is excited and the inductance calculated from the current through the port. Solving analytically and taking into account that $M = k\sqrt{L_1L_2}$, we arrive at the following expressions which we can derive the modeling error from:

$$L_3 = L_1(1 - k^2) \tag{5}$$
$$L_4 = L_2(1 - k^2) \tag{6}$$

From (5), and (6) it can be seen that the error is equal to $-k^2$. The error quickly grows as the coupling increases, but is limited for small coupling.

However, in practice the least squares error of the system is minimized when extracting parameters. During the extraction process, we excite each port in turn and measure the resulting currents. Each set of values are substituted to combined to form a set of equations that can be solved. These equations are solved using the least squares method.

$$\begin{bmatrix} \frac{1}{L_1(1-k^2)} & 0 \\ 0 & \frac{k}{\sqrt{L_1L_2}(1-k^2)} \\ \frac{k}{\sqrt{L_1L_2}(1-k^2)} & 0 \\ 0 & \frac{1}{L_2(1-k^2)} \end{bmatrix} \cdot \begin{bmatrix} L_3 \\ L_4 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 1 \end{bmatrix} \tag{7}$$

The least squares solution of equations in (7) can be obtained analytically:

$$L_3 = \frac{L_1(1 - k^2)}{1 + \frac{L_1}{L_2}k^2} \tag{8}$$
$$L_4 = \frac{L_2(1 - k^2)}{1 + \frac{L_2}{L_1}k^2} \tag{9}$$

The comparison between the accuracy of the least squares solution and the trivial case is shown in Fig. 3. It can be seen that the error from the least squares solution is greater than the error from the trivial case.

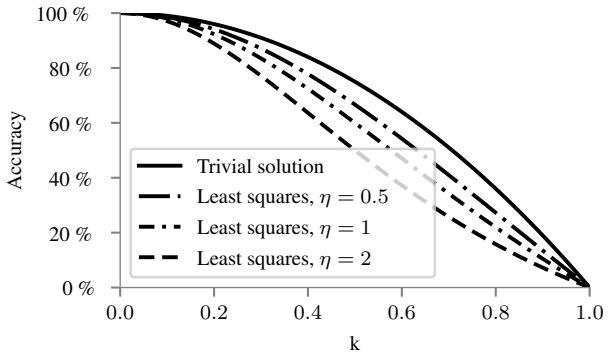

Fig. 3. Self-inductance accuracy, where η is the ratio between the extracted and coupled inductor.

If multiple mutual inductances are ignored the self-inductance error is compounded. It is now abundantly clear that ignoring mutual coupling in the extraction process leads to incorrect self-inductance values. Whether this is desirable is dependent on the user or the application. It is important to point out that this is not a reflection on the inductance extraction method. The method has to extract a model for a system, which may not be accurately described through the model. The resulting model minimizes the least squared error of the system.

III. Singular value problem

The intuitive solution to the before-mentioned problem is to add mutual coupling between all inductors. However, this leads to other problems. In a highly coupled netlist, the parameter extraction equations matrix is often ill-conditioned. The least-squares solution can still be found by disregarding the singular values that are close to or equal to zero when constructing the pseudo-inverse. However, this can lead to unrealistically large mutual inductances, negative inductances, and even coupling factors that are greater than one. This is, again, not a problem with the method, but with the model. The additional mutual inductances lead to an under-constrained problem. There are multiple different solutions, of which the least square solution is one.

To illustrate the root cause of the singular value problem, we analyze the most basic case on which the problem can be illustrated. Fig. 4 shows the simplest case, an inductance star network.

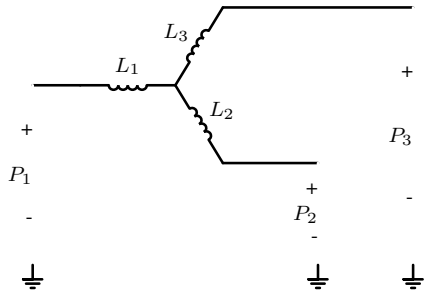

Fig. 4. Inductance star network.

During the extraction process, we excite each port in turn and measure the resulting currents. Given the port currents, we have enough information to determine the current distribution of the entire star network. We can then construct the equations required to solve the inductances.

$$0 = V(P_1) - V(L_1) + V(L_2) - V(P_2) \tag{10}$$
$$0 = V(P_1) - V(L_1) + V(L_3) - V(P_3) \tag{11}$$
$$0 = V(P_3) - V(L_3) + V(L_2) - V(P_2) \tag{12}$$

We can see that (12) = (10) − (11). Since (12) is a linear combination of (10) and (11), we can disregard (12) as it is implied by (10) and (11). We can then simplify (10), (11), and (12) to:

$$0 = V(P_1) - j\omega L_1 I_1 + j\omega L_2 I_2 - V(P_2), \text{ and} \tag{13}$$
$$0 = V(P_1) - j\omega L_1 I_1 + j\omega L_3 I_3 - V(P_3). \tag{14}$$

Substituting the current and voltage values of each excitation into (13) and (14) gives us six equations. Solving these six equations gives us the inductance values.

Setting aside, for a moment, the previous example, we analyze a similar circuit wit the same port structure, but a different inductance network. The circuit is shown in Fig. 5.

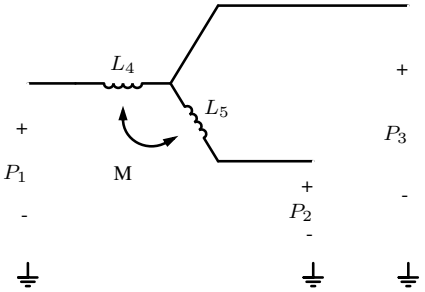

Fig. 5. Inductance star alternative network.

Following the same procedure as earlier, we arrive at the following equations:

$$\begin{aligned} 0 = {} & V(P_1) - j\omega L_4 I_1 + j\omega M I_2 \\ & + j\omega L_5 I_2 - j\omega M I_1 - V(P_2) \end{aligned} \tag{15}$$
$$0 = V(P_1) - j\omega L_4 I_1 + j\omega M I_2 - V(P_3) \tag{16}$$

Given that $I_3 = -I_1 - I_2$ holds, we substitute

$$L_4 = L_1 + L_3 \tag{17}$$
$$L_5 = L_2 + L_3 \tag{18}$$
$$M = -L_3 \tag{19}$$

into (15) and (16), simplify, then we get back to (13) and (14). Similarly, we can substitute

$$L_1 = L_4 + M \tag{20}$$
$$L_2 = L_5 + M \tag{21}$$
$$L_3 = -M \tag{22}$$

into (13) and (14), simplify, and get (15) and (16). From this, we can infer that there is a one-to-one mapping between the two networks.

Both Fig. 4 and Fig. 5 are special cases of the fully coupled star network shown in Fig. 6.

If a solution with no mutual coupling exists then, there also exists a solution with $L_8 = 0$, and another solution with $L_6 = 0$, and another with $L_7 = 0$. The solution to the linear set of equations used to determine the inductances are therefore underdetermined.

An inductive network distributes current given a phase excitation similarly to how a resistive network distributes current given a voltage distribution [8]. This follows intuitively from looking at the similarities between $\frac{\Phi_0 \phi}{2\pi} = IL$ and $V = IR$. For a resistive network to be able to distribute current in an arbitrary distribution three degrees of freedom, given by the resistor values, are required. An arbitrary current distribution

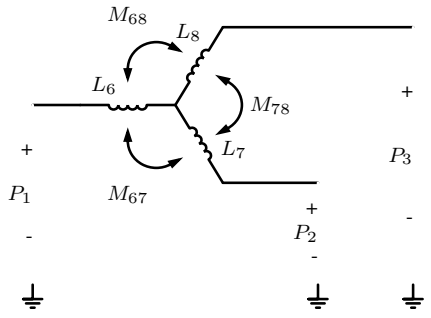

Fig. 6. Fully coupled inductance star network.

can, therefore, be realized by the three inductors. Given the additional three degrees of freedom, from the mutual coupling, we can write the solution set as:

$$\begin{bmatrix} L_6 \\ L_7 \\ L_8 \\ M_{67} \\ M_{78} \\ M_{68} \end{bmatrix} = \begin{bmatrix} L_1 \\ L_2 \\ L_3 \\ 0 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} -L_1 & L_2 & L_3 \\ L_1 & -L_2 & L_3 \\ L_1 & L_2 & -L_3 \\ 0 & 0 & -L_3 \\ -L_1 & 0 & 0 \\ 0 & -L_2 & 0 \end{bmatrix} \cdot \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{23}$$

where a, b, and c can be any real value. Substituting (23) into (10), and (11) we get (13), and (14). Given the solution set, one can easily show that negative inductances and coupling factors greater than one are possible. The underconstrained and possibly non-physical solution is indicative of a modeling error.

IV. Algorithm

Consider a circuit which has the minimum number of inductors to represent a circuit fully. We call a set of inductors that fully represent a circuit a fundamental inductor set (FIS). All possible inductive loops can be represented by taking a linear combination of effects of the given fundamental inductor set. A cycle with only a single inductance requires that the inductance represents the cycle for the cycle to have the correct self-inductance. Each inductor is therefore analogous to a cycle in a fundamental cycle basis (FCB) of the circuit graph. A circuit graph can have more than one FCB [9]. Different FCBs can form different sets of minimum inductors. Every fundamental inductance set has a parameter solution that exactly matches the pure inductive network. We only need to find one fundamental inductor set for a circuit.

An FCB is constructed by taking the edges not in the corresponding spanning tree and the path linking the two end points [9]. The inductors of a minimum inductor set correspond to the edges not in the corresponding spanning tree.

We have developed two algorithms that can be used to determine the minimum inductance set of a superconducting circuit. The first uses a Breadth-First Search (BFS) algorithm [9], and the second uses the Disjoint Set data structure [9]. For terminology we refer readers to [9], but any undergraduate graph theory textbook will be sufficient.

A. BFS

A BFS is performed on a circuit graph. If a tree-edge is an inductor, the inductor must be removed and the two connected nodes short-circuited. This ensures that there is no inductors part of the spanning tree. If a non-tree-edge is not an inductor, an inductor should be added in series to the edge. This ensures that a spanning tree exists where the non-tree edges are all inductors. Together this ensures that all inductors in the circuit graph form a fundamental inductor set.

The algorithm could potentially rearrange existing inductors even if the initial inductor set is fundamental. Rearranged inductances are not a problem if only used as a simulation model, but a designer will benefit from having a fixed circuit layout. The before mentioned problem can be solved by always visiting a non-inductive edge if such an edge exists and only visiting inductive edges if no alternative edges can be visited. If a circuit contains a fundamental inductance set, then the inductive-edges will all fall on non-tree edges, and the spanning tree will contain only non-inductive edges, which ensures that no inductors will be added or removed.

This algorithm can be implemented in $\mathcal{O}(E)$ time complexity and $\mathcal{O}(V+E)$ space complexity. V is the number of voltage nodes in the circuit graph, and E is the number of edges in the circuit graph.

B. Disjoint Set

A disjoint set data structure is created where each voltage node is initially in its own set. Each edge of the circuit graph is iterated over. Each edge is checked if it is a non-tree or tree edge by examining whether the two connecting nodes of the edge is in the same set. If the two connecting nodes are in the same set, then the edge is a non-tree edge; otherwise, it is a tree edge. The same procedure is followed as with the BFS where inductive non-tree-edges are removed, and inductors are added in series on non-inductive tree-edges. After an edge is processed, the connecting node sets are unioned.

To address the issue of rearranged inductances: All non-inductive edges should be processed before the inductive edges. As with the BFS algorithm, this ensures that all non-tree edges will not be inductive and tree edges will be inductive if a fundamental inductor set is given.

This algorithm can be implemented in $\mathcal{O}(\alpha(V)E)$ time complexity and $\mathcal{O}(V)$ space complexity, where α is the inverse Ackermann function.

C. Application

Both algorithms give accurate results and are fast and space-efficient enough to work on very large scale circuits. We prefer the Disjoint Set variant over the BFS variant as we found the implementation to be much simpler.

We illustrate a fundamental inductor set by investigating a Josephson Transmission Line (JTL). Fig. 7 shows a JTL with inductors on each segment. Fig. 7 is how a circuit designer will model the inductive network if no mutual couplings is taken into account. If the mutual inductance is negligible then the inductive circuit will accurately be modeled by inductor on each

segment with no mutual coupling. Unfortunately the mutual inductance is almost never negligible in layed out cells.

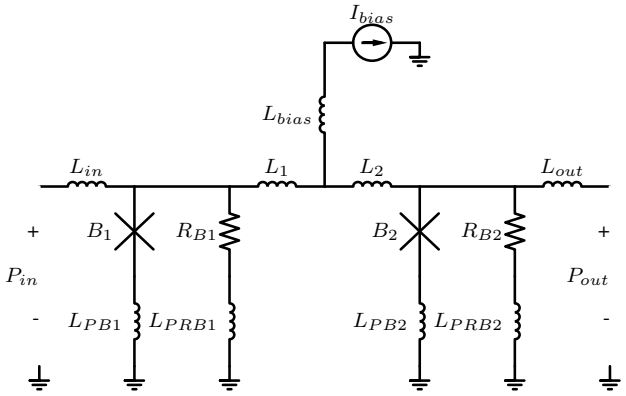

Fig. 7. JTL circuit diagram with inductors on each segment.

If the fundamental inductor set is used and coupling is assumed between all inductors, then an inductive circuit will be modeled accurately even in the presence of strong mutual inductances. Fig. 8 shows the JTL, but with a fundamental inductor set. The circuit graph in Fig. 8 is a possible output of both algorithms. The actual output of the algorithms will vary based on the edge ordering and, in the case of the BFS, the starting node. The equations resulting from inductance extraction will not be singular and will exactly model pure inductive circuits.

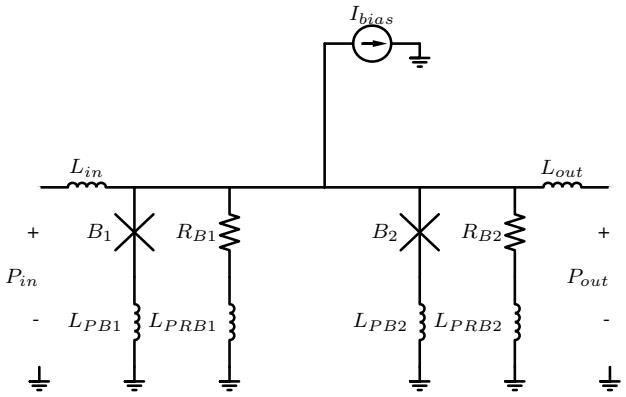

Fig. 8. JTL circuit diagram with a possible minimum inductor set.

Table I shows the cycles that are represented by each inductor in the fundamental inductor set of the circuit shown in Fig. 8. All other cycles in the circuit graph can be made from a linear combination of the cycles since the cycles form an FCB.

V. Circuit Design

The fundamental inductor set accurately models a circuit but does not directly map to the common mental model which most designer use during superconductor electronic design. The common mental model is that inductors are seen as segments. The error that can be introduced by not fully modeling mutual coupling is too large to ignore.

This section will discuss how the fundamental inductance model influences the superconductor circuits and their designs.

TABLE I
Cycles represented by inductors in the fundamental inductor set.

Inductor	Edges in cycle represented by inductor
Lin	Pin, Lin, Ibias
LPB1	LPB1, B1, Ibias
LPRB1	LPRB1, RB1, Ibias
LPB2	LPB2, B2, Ibias
LPRB2	LPRB2, RB2, Ibias
Lout	Pout, Lout, Ibias

A. Arbitrary loop inductances

The loops the minimum inductor set compromises of are not necessarily the loops used in the design. We show how to determine the self-inductance of any loop, and the mutual inductance of any two loops in a circuit.

To determine the mutual inductance of any two loops, one assumes that the change in current, $\frac{di}{dt}$, around the loop is one and that that is the only change in current in the circuit. The induced voltage around the other loop is then the mutual inductance of the two loops. The self-inductance is determined by the same procedure, but the excited and measured loop is taken as the same loop.

B. Unexcited current loops

A fundamental inductance set corresponds to a fundamental cycle basis of the circuit. Integrating the phase around the n fundamental cycles, KVL, formed by a fundamental inductance set we arrive at

$$\frac{\phi_i \Phi_0}{2\pi} = \sum_j L_{j,i} I_j \; \forall \; i = \{1, \ldots, n\}, \tag{24}$$

where ϕ_i is the phase over the ith fundamental inductor, and $L_{i,i}$ is the self inductance of the ith fundamental inductor, and $L_{i,j}$ is the mutual inductance between the ith and jth fundamental loop, i_j is the current through the j fundamental inductor and n is the number of fundamental inductance loops. Equation (24) can be neatly written in matrix notation

$$\begin{bmatrix} \frac{\phi_1 \Phi_0}{2\pi} \\ \vdots \\ \frac{\phi_n \Phi_0}{2\pi} \end{bmatrix} = \begin{bmatrix} L_{1,1} & \cdots & L_{1,n} \\ \vdots & \ddots & \vdots \\ L_{n,1} & \cdots & L_{n,n} \end{bmatrix} \begin{bmatrix} I_1 \\ \vdots \\ I_n \end{bmatrix}. \tag{25}$$

In a circuit, there are possible unexcited loops. These unexcited loops can result from holes which have no trapped flux, grounded ports, or negligible excitations. Rewriting (25) into block matrix notation

$$\begin{bmatrix} \frac{\phi_e \Phi_0}{2\pi} \\ \mathbf{0} \end{bmatrix} = \begin{bmatrix} \mathbf{L}_{e,e} & \mathbf{L}_{e,u} \\ \mathbf{L}_{u,e} & \mathbf{L}_{u,u} \end{bmatrix} \begin{bmatrix} \mathbf{I}_e \\ \mathbf{I}_u \end{bmatrix} \tag{26}$$

where ϕ_e is the fundamental loop phase excitations, and the subscript e and u refers to the excited and unexcited parts of the equation. Equation (26) can be simplified to

$$\left[\frac{\phi_e \Phi_0}{2\pi}\right] = \left[\mathbf{L}_{e,e} - \mathbf{L}_{e,u}\mathbf{L}_{u,u}^{-1}\mathbf{L}_{u,e}\right]\left[\mathbf{I}_e\right] \tag{27}$$

This means that any unexcited loop or holes can be accounted for by calculating an effective inductance of the excited loops. Unfortunately, any superconductor loop can be a source of excitation since all superconductor loops can potentially trap flux, flux trapping is outside the scope of this paper. We refer any interested readers to [10] for a reference article on flux trapping.

C. Adiabatic Quantum Flux Parametron (AQFP) [11], [12]

For a reference analysis we investigate the AQFP NOT gate [13] designed for the MITLL SFQ5ee process [14] [15]. The traditional circuit is shown in Fig. 9. Coupling is taken into account between L_{dc} and L_q, L_x, L_{out}, L_1, and L_2 is taken into account as well as the coupling between L_x, and L_{out}, L_q, L_1, L_2, and between L_{out} and L_q. The InductEx extraction resulted in a $7.28\ \%$ error.

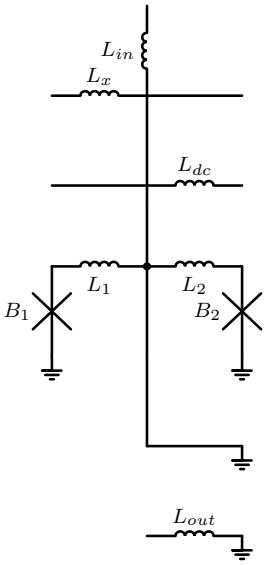

Fig. 9. Normal AQFP NOT gate designed for the MITLL SFQ5ee process.

In Fig. 10 the AQFP gate with a fundamental inductance set is shown. Coupling is included between all fundamental inductors. The InductEx extraction resulted in a $0.02\ \%$ error.

Assuming that the model is symmetrical, and that numerical error is the cause of asymmetry, looking only at the inductance of the SQUID loop, the coupling between the SQUID loop to ground (L_q in the normal representation and M_{12} in the fundamental representation), and assuming the output inductor contribution to the potential energy is negligible we can calculate β_l and β_q of the network for both the normal [12]

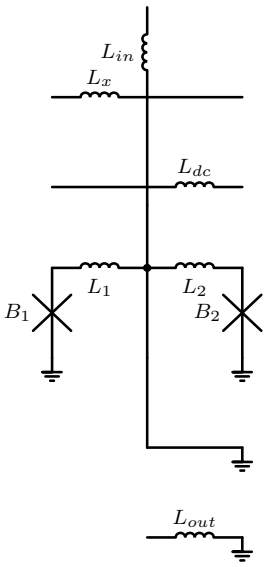

Fig. 10. Fundamental AQFP NOT gate designed for the MITLL SFQ5ee process.

$$\beta_l = \frac{\pi I_c}{\Phi_0}\left(L_1 + L_2\right) \text{ and} \tag{28}$$

$$\beta_q = \frac{2\pi I_c}{\Phi_0}\left(L_q\right), \tag{29}$$

and fundamental case

$$\beta_l = \frac{\pi I_c}{\Phi_0}\left(L_1 + L_2 - 2M_{12}\right) \text{ and} \tag{30}$$

$$\beta_q = \frac{2\pi I_c}{\Phi_0}\left(M_{12}\right). \tag{31}$$

Table V-C tabulates the results. It is clear that the extraction error does lead to a corresponding error in circuit parameters.

	Normal	Fundamental	Percentage error
β_l	0.249	0.267	6.78%
β_q	0.951	0.933	2.00%

TABLE II
SIMPLIFIED MODELING OF INDUCTANCES.

However, the effect of the output inductor and it is coupling to the circuit is not taken into account in the above estimation. In the normal mode system the output inductor does not couple with the SQUID loop and only couples significantly with L_q. Also, in practice the output inductor is connected to another circuit. We model this connection by adding a inductive load, L_{load} which does not couple to the system. By assuming the output does not provide feedback to circuit the effective β_q, which we denote β_q^* can be calculated as

$$\beta_q^* = \frac{2\pi I_c}{\Phi_0}\left(L_q - \frac{M_{out,q}^2}{L_{out}+L_{load}}\right). \tag{32}$$

The effective parameters, β_q^* and β_l^* can also be calculated for the fundamental case as

$$\beta_q^* = \frac{2\pi I_c}{\Phi_0}\left(M_{12} - \frac{M_{1out}M_{2out}}{L_{load}+L_{out}}\right), \text{and} \tag{33}$$

$$\beta_l^* = \frac{\pi I_c}{\Phi_0}\left(L_1 + L_2 - 2M_{12} - \frac{(M_{1out}-M_{2out})^2}{(L_{load}+L_{out})}\right). \tag{34}$$

This is a rare case where a parasitic effect is beneficial to the system. The output inductor lowers the effective inductance of the SQUID to ground. By lowering the output load, the energy efficiency of the AQFP gate improves along with the current gain. The case where the output load does not make a difference is when L_{load} becomes infinitely large. However, since L_{load} corresponds to a worst-case scenario, it is not a mistake to ignore the effect of the load when estimating the effective inductance parameters of the circuit.

If we assume that the model is symmetrical and that any asymmetry is numerical error then the standard potential equation [16] for QFP can be used.

$$U(\phi_+, \phi_m) = \frac{E_J}{2\pi}\left[\frac{(\phi_x-\phi_-)^2}{\beta_l} + \frac{(\phi_i n-\phi_+)^2}{\beta_l+2\beta_q}+\right] \tag{35}$$

Unfortunately, practice is seldom symmetrical. We proceed to calculate the energy in the case of an asymmetric QFP.

By using the same normalization as the standard case uses the input currents are defined as

$$I_{in} = \frac{\Phi_0\phi_{in}}{\pi\left(M_{in1}+M_{in2}\right)}, \text{and} \tag{36}$$

$$I_{dc} = \frac{\Phi_0\phi_{dc}}{\pi\left(M_{dc1}-M_{dc2}\right)}, \text{and} \tag{37}$$

$$I_x = \frac{\Phi_0\phi_x}{\pi\left(M_{x1}-M_{x2}\right)}. \tag{38}$$

The currents in the branches can be calculated from the common, ϕ_+ and difference ϕ_- phases.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} L_1 & M_{12} \\ M_{12} & L_2 \end{bmatrix}^{-1} \cdot \begin{bmatrix} \frac{\Phi_0(\phi_+ + \phi_-)}{2\pi} \\ \frac{\Phi_0(\phi_+ - \phi_-)}{2\pi} \end{bmatrix} \tag{39}$$

With the currents the flux contribution from all current source can be calculated.

$$\begin{bmatrix} \Phi_1 \\ \Phi_2 \end{bmatrix} = \begin{bmatrix} M_{x1} & M_{dc1} & M_{in1} & L_1 & M_{12} \\ M_{x2} & M_{dc2} & M_{in2} & M_{12} & L_2 \end{bmatrix} \cdot \begin{bmatrix} I_x \\ I_{dc} \\ I_{in} \\ I_1 \\ I_2 \end{bmatrix} \tag{40}$$

The energy in the inductance network can be calculated using the magnetic flux in the inductor network.

$$U_L = \mathbf{\Phi}^T \mathbf{L}^{-1} \mathbf{\Phi}. \tag{41}$$

The potential of the QFP gate becomes

$$U_{QFP} = U_L - \frac{\Phi_0^2 cos\left(\phi_+ + \phi_-\right)}{L_J} - \frac{\Phi_0^2 cos\left(\phi_+ - \phi_-\right)}{L_J}. \tag{42}$$

It should be noted that 42 reduces to the symmetric form, (35), when the parameters are symmetrical. We verified this by using sympy [17], a computer algebra system, to avoid a mistakes when working with the long equations. The symmetrical conditions are listed below.

$$L_1 := L^* + L_q \tag{43}$$
$$L_2 := L^* + L_q \tag{44}$$
$$M_{12} := L_q \tag{45}$$
$$M_{dc1} := M_{dc}^* \tag{46}$$
$$M_{dc2} := -M_{dc}^* \tag{47}$$
$$M_{in1} := M_{in}^* \tag{48}$$
$$M_{in2} := M_{in}^* \tag{49}$$
$$M_{x1} := M_x^* \tag{50}$$
$$M_{x2} := -M_x^* \tag{51}$$
$$\tag{52}$$

The potential energy plot for the asymmetric QFP and symmetric QFP is plotted in Fig. 12 and Fig.11. The difference is minimal as the layout is, in fact, geometrically symmetrical and the asymmetry is a result of numerical error. The asymmetric expression will, however, be useful when developing more compact asymmetrical gates.

We have shown that, for QFP, the extraction error resulting from neglecting parasitic coupling leads to a corresponding error in design parameters. This parasitic coupling should be taken into account when performing software verification of designs.

D. Rapid Single Flux Quantum (RSFQ) [18]

We investigate the bias currents of a simple Passive Transmission Line (PTL) [19] repeater. Our PTL repeater is a simple three junction Josephson transmission line. The normal representation is shown in Fig. 13, and a fundamental representation is shown in Fig. 14.

As our study is on the fundamental inductances and not on circuit design, we assume that all design aspects is a priori knowledge. The loop inductances, L_1, and L_2, the junction critical currents, I_{C1}, I_{C2}, and I_{C3}, and junction bias currents, I_{B1}, $I_{B2}4$, and I_{B3}, are, therefore, considered predetermined constants. The parasitic kinetic inductances, L_{p1}, L_{p2}, and L_{p3} are also considered to be know from process information.

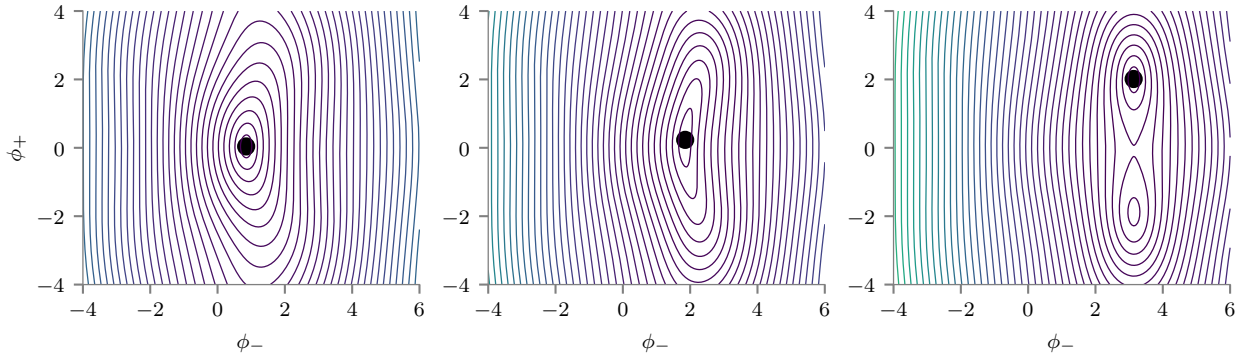

Fig. 11. Symmetric AQFP potential energy plot.

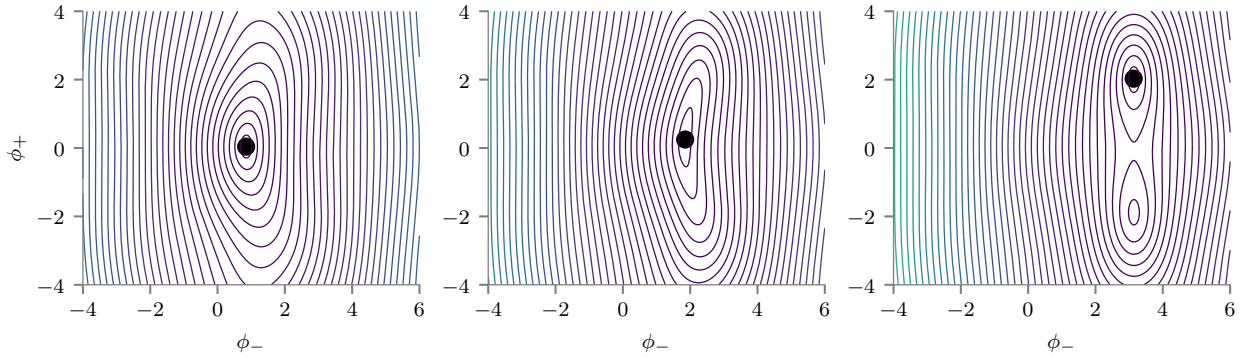

Fig. 12. Asymmetric AQFP potential energy plot.

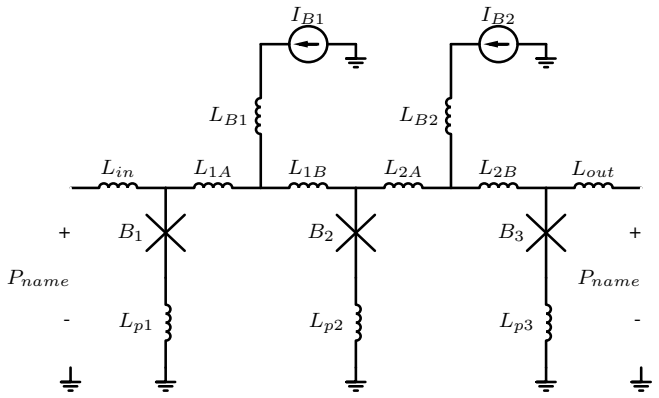

Fig. 13. Normal PTL repeater netlist.

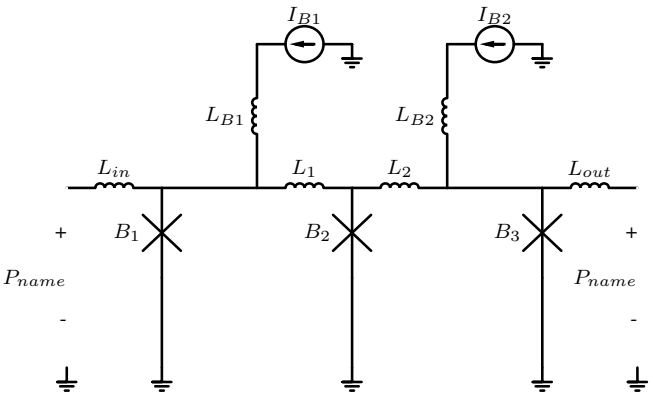

Fig. 14. Fundamental PTL repeater netlist.

The current flowing in L_1, L_2, L_{B1}, and L_{B2} is defined as I_{L1}, I_{L2}, I_{B1}, and I_{B2} respectively. Given the current definitions we can write down the currents through the junctions.

$$I_{J1} = I_{B1} - I_{L1} \tag{53}$$
$$I_{J2} = I_{L1} - I_{L2} \tag{54}$$
$$I_{J3} = I_{L2} + I_{B2} \tag{55}$$

Equations (53), (54), and (55) implies that the sum of the two current sources equal to the sum of all the currents through the

junctions.

$$I_{B1} + I_{B2} = I_{J1} + I_{J2} + I_{J3} \tag{56}$$

The implication of (56) might seem intuitive, but since the information is included in (53), (54), and (55), it does not need to be explicitly considered.

Given that each current source provides current to half of the circuit, we choose that the first current source should provide enough current to bias the first junction and half of the second junction.

$$I_{B1} = I_{J1} + \frac{1}{2} I_{J2} \tag{57}$$

Equation (57) along with (56) implies that the second current source provides enough current to bias the third junction and half of the second junction.

$$I_{B2} = \frac{1}{2} I_{J2} + I_{J3} \tag{58}$$

Equation (53) and (55) now be manipulated to get equations for the currents in through the two inductors:

$$I_{L1} = \frac{1}{2} I_{J2} \tag{59}$$

$$I_{L2} = -\frac{1}{2} I_{J2} \tag{60}$$

All currents in the system are now defined, and we continue by calculating the phase over the inductors.

$$\begin{bmatrix} \phi_{L1} \\ \phi_{L2} \end{bmatrix} = \begin{bmatrix} L_1 & M_{1,2} & M_{1,B1} & M_{1,B2} \\ M_{1,2} & L_2 & M_{2,B1} & M_{2,B2} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{B1} \\ I_{B2} \end{bmatrix} \tag{61}$$

Applying KVL on the loops formed by the fundamental inductors we arrive at a set of equations we can use to solve the fundamental inductances and their coupling.

$$0 = -\sin^{-1}\left(\frac{I_{J1}}{I_{C1}}\right) + \phi_1 + \sin^{-1}\left(\frac{I_{J2}}{I_{C2}}\right) \tag{62}$$

$$0 = -\sin^{-1}\left(\frac{I_{J2}}{I_{C2}}\right) + \phi_2 + \sin^{-1}\left(\frac{I_{J3}}{I_{C3}}\right) \tag{63}$$

$$\tag{64}$$

Here we would like to draw attention to the fact that we have more unknowns than equations. This is because some of the mutual couplings are purely parasitic. The mutual inductances $M_{1,B2}$ and $M_{2,B1}$ are purely magnetic inductances. We continue by assuming that the parasitic magnetic inductances are negligible in our PTL repeater. The mutual coupling between the two transmission loops, M_{12}, is a result of the parasitic kinetic inductance, L_{p2} between the loops.

$$M_{1,2} = -L_{p2} \tag{65}$$

$$M_{1,B2} = 0 \tag{66}$$

$$M_{2,B1} = 0 \tag{67}$$

With the parasitic parameters accounted for, equation (62), and (63) can be solved.

$$M_{2,B2} = \frac{\pi I_{L1} L_{p2} - \pi I_{L2} L_2 + \frac{\Phi_0 \operatorname{asin}\left(\frac{I_{J2}}{I_{C2}}\right)}{2} - \frac{\Phi_0 \operatorname{asin}\left(\frac{I_{J3}}{I_{C3}}\right)}{2}}{\pi I_{B2}} \tag{68}$$

$$M_{1,B1} = \frac{-\pi I_{L1} L_1 + \pi I_{L2} L_{p2} + \frac{\Phi_0 \operatorname{asin}\left(\frac{I_{J1}}{I_{C1}}\right)}{2} - \frac{\Phi_0 \operatorname{asin}\left(\frac{I_{J2}}{I_{C2}}\right)}{2}}{\pi I_{B1}} \tag{69}$$

Since there is no parasitic magnetic inductance in the design, we can define the loop inductances and their coupling in terms of the branch inductors.

$$L_1 = L_{p1} + L_{1A} + L_{1B} + L_{p2} \tag{70}$$

$$L_2 = L_{p2} + L_{2A} + L_{2B} + L_{p3} \tag{71}$$

$$M_{1,B1} = -L_{2B} - L_{p3} \tag{72}$$

$$M_{2,B2} = L_{p1} + L_{1A} \tag{73}$$

Equations (70), (71),(72), and (73) can be re-arranged to give expressions of the branch inductances in terms of the loop inductances and their coupling.

$$L_{1A} = -L_{p1} - M_{1,B1} \tag{74}$$

$$L_{1B} = L_1 - L_{p2} + M_{1,B1} \tag{75}$$

$$L_{2A} = L_2 - L_{p2} - M_{2,B2} \tag{76}$$

$$L_{2B} = -L_{p3} + M_{2,B2} \tag{77}$$

In the parasitic free case, the design can be done directly with the branch currents and arrive at the same equations. However, in the fundamental case, explicit attention had to be given to the parasitic coupling. This explicit attention is important as it informs the designer of potential coupling that can happen between loops when laying out the circuit. It also gives parameters, which, when extracted, gives the circuit designer an indication of the parasitic coupling taking place. Furthermore, if the parasitic coupling is unavoidable, then the parasitic coupling can be taken into account in the design by using a fundamental inductance representation. The fundamental inductance representation is, therefore, invaluable for designing circuits with potential parasitic coupling.

E. Superconductor Quantum Interference Device (SQIF) [20]

Superconducting quantum interference devices (SQUIDs) are extremely sensitive magnetometers. They consist of a superconducting loop with 1 (RF-SQUID) or 2 (DC-SQUID) Josephson junctions in the superconducting loop. To improve

sensitivity and dynamic range, they can be stacked in 2D arrays. SQUID array of SQIF design is a topic on its own, and we will not delve into it. We will, however, look at a common assumption, that loops have negligible magnetic coupling, often made during SQIF design [20], [21].

We extracted the inductance of virtual test structures which represents a basic SQUID array with varying number of loops. For each test structure, we extracted the inductance using the per-segment and fundamental approach. As an illustration of how the netlists of the SQUID arrays look Fig 15 shows the schematic of the 3x3 SQUID array using the per-segment inductance model and Fig. 16 shows the schematic of the 3x3 SQUID array using the fundamental inductance model.

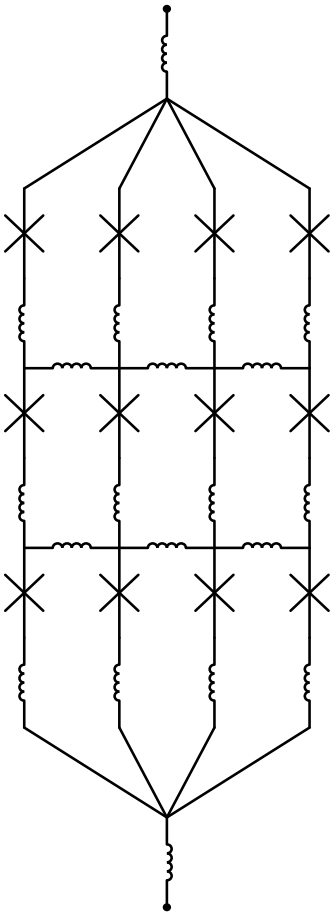

Fig. 15. Normal representation of 3x3 SQUID array.

Table V-E shows the extraction results of the various test structures. The per-segment inductance values are accurate for the single SQUID loop, but quickly lose accuracy as more loops are added. The fundamental inductance values remain at least as accurate as of the tolerance of the 3D simulation.

It is clear that neglected coupling in the SQUID arrays

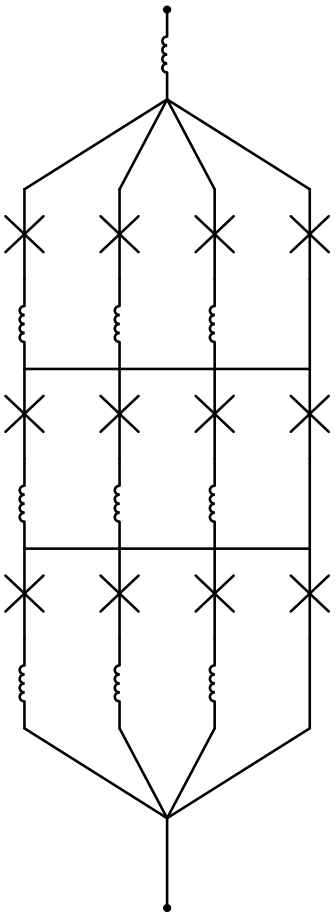

Fig. 16. Fundamental representation of 3x3 SQUID array.

Array size	Segment accuracy	Fundamental accuracy
1x1	> 99.9 %	> 99.9 %
2x2	82.9 %	> 99.9 %
3x3	66.3 %	> 99.9 %
4x4	60.9 %	> 99.9 %
5x5	58.3 %	> 99.9 %

TABLE III
ACCURACY OF INDUCTANCE EXTRACTION OF SQUID ARRAYS OF VARIOUS SIZES.

leads to unreliable extracted parameters. From looking at the potential loop coupling, it is also clear that the bias line can couple with the inner SQUID loops. This can cause the bias currents of the junctions to drift from their expected values significantly.

The per-segment inductance model is unsuitable for any meaningful SQUID array calculations. We want to note the SQUID structures can be affected by resonances in the structure which are not accounted for in the fundamental inductance model. As such, we will conclude that the fundamental inductance model gives a much more accurate simulation model

of SQUID arrays, but it does not describe all electromagnetic effects of interest. It does give a solid foundation on which to extend the SQUID array simulation model to be encompassing all effects of interest.

VI. Conclusion

We have analyzed two significant causes of inductance extraction errors. We have shown that ignoring mutual inductance leads to incorrect self-inductances. We have also shown that adding too many inductors leads to exactly singular matrices during the extraction process. The Fundamental inductance representation was proposed, which solves both the aforementioned problems. The effect of parasitic and asymmetric coupling on an AQFP gate was analyzed. A loop-based design of a PTL repeater was shown to show how parasitics influence RSFQ design. We have shown that parasitic coupling introduces significant modeling errors in SQIFs. We have shown several examples of how a fundamental inductance model significantly improved inductance extraction accuracy. We conclude that the fundamental inductance model is essential in verifying superconductor circuits and designing circuits with parasitics.

VII. Acknowledgments

We would also like to thank Prof. Yoshikawa, Chris Ayala, and Olivia Chen, for allowing us to use the AQFP MITLL cell library for this publication. We would also like to thank Pascal Fevbre for the insight that SFQ logic cells are an arrangement of SQUID loops and that the designer should consider the loops in the circuit.

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Appendix D

Journal Paper: JoSIM-Superconductor SPICE Simulator

- J. A. Delport, K. Jackman, P. l. Roux and C. J. Fourie, "**JoSIM-Superconductor SPICE Simulator**," in IEEE Transactions on Applied Superconductivity, vol. 29, no. 5, pp. 1-5, Aug. 2019

The majority of the contributions to this article are from the co-authors. I made minor contributions to the JoSIM codebase. I specifically contributed a minor performance optimization, made improvements to the build scripts, and implemented the python bindings. IEEE Transactions on Applied Superconductivity hold the copyright for this article.

JoSIM—Superconductor SPICE Simulator

Johannes Arnoldus Delport, *Student Member, IEEE*, Kyle Jackman, Paul le Roux, *Student Member, IEEE*, and Coenrad Johann Fourie, *Senior Member, IEEE*

***Abstract*—We present Josephson simulator (JoSIM), a simulation program with integrated circuit emphasis (SPICE)-based circuit simulator that utilizes the modified nodal voltage analysis method and trapezoidal integration to solve systems of linear equations. The objective of JoSIM is to provide accurate simulation results with major improvement in terms of simulation speed and expandability. JoSIM incorporates the ability to do phase-based simulation through a modified nodal phase analysis method. A full data visualization GUI, built using open-source graphical libraries, is included. We show the results of simulations with JoSIM and compare them to the results of the JSIM, as well as comparisons between simulation times. We also show extremely large simulations, which are not realizable in reasonable time using JSIM.**

***Index Terms*—Circuit analysis, circuit simulation, Josephson junctions, SPICE, superconducting integrated circuits.**

I. Introduction

SIMULATION program with integrated circuit emphasis (SPICE) simulation in superconductivity is a rather niche field due to difficulty in representing the actual physics of the Josephson junction (JJ) element in terms of circuit models for simulation [3]. Most simulators rely on approximations such as the resistively and capacitive shunted junction (RCSJ) to model the tunnel current effect of the JJ [4]. Despite being approximations, the modelled effect is suitable for simulation purpose and near enough to practical results to be acceptable in most cases. The closest approximation of the Josephson junction that models the Josephson effect most accurately was done by Werthamer in 1966 [5]. This model though has not seen exact implementation in a general simulation engine, with the closest being the microscopic tunnel junction (MTJ) in the personal superconductor circuit analyser (PSCAN) [6].

Simulation of the Josephson effect had been possible through model additions to Berkeley SPICE and IBM ASTAP, though the first published attempt at the Josephson effect in simuation program with integrated circuit emphasis (SPICE) was by Jewett at University of California Berkeley in 1982 [7]. The JJ model was added to the existing SPICE 2G5 and allowed the user to choose one of 3 types of quasiparticle resistances (Rtype). This method was however rather slow due to the numerical method used by SPICE for accurate simulation of transistor type devices. The SPICE 2G5 with the implementation of the JJ was named JSPICE, with the SPICE3 version JSPICE3 as its successor [8].

WRspice is a SPICE engine developed by Whiteley Research Incorporated in Sunnyvale, CA. Until October of 2017 it was a commercial SPICE engine and part of a toolset called XicTools, which included the layout package Xic. Development started as a project to rewrite JSPICE3 in C++ while maintaining full compatibility for older SPICE simulators.

Josephson simulator (JSIM) [9] developed by Fang and Van Duzer in 1989 is a SPICE-like simulator dedicated to simulation of JJs and does not support any semiconductor devices. The simulator is very light weight due to the need to only support a few components.

In this paper we present JoSIM, a Josephson junction SPICE simulation engine for transient analysis akin to JSIM and WRspice written in modern C++ with emphasis on extendibility while remaining focused on superconductive circuit elements.

We compare JoSIM to JSIM and WRspice in terms of accuracy of the JJ model and execution speed of various size simulations.

II. Simulation Engine

At the core of any simulation engine lies the process of finding a set of equations that can be simultaneously solved for either a fixed point (static) solution or a transient solution (time dependant). In circuit simulation Kirchoff's current law (KCL) is used to do nodal analysis to find the voltages at each node, however it is often difficult to do without information about the branch currents and therefore modified nodal analysis (MNA) [10] is used to set up these equations.

Reactive components such as inductors and capacitors require some form of integration method to determine the current or voltage at every time step. The most basic of these methods is the backward Euler method, which interpolates the current value based on the previous value. This method is however a first order method which does not model the behaviour accurately enough unless sufficiently small time steps are taken which quickly becomes computationally expensive. We therefore opt to use a second order method such as the trapezoidal integration method. Trapezoidal integration method is defined as

$$\left.\frac{dy}{dt}\right|_n = \frac{2}{h_n}\left(y_n - y_{n-1}\right) - \left.\frac{dy}{dt}\right|_{n-1} \tag{1}$$

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The authors are with the Department of Electrical and Electronic Engineering, Stellenbosch University, Stellenbosch 7602, South Africa (e-mail: joeydelp@gmail.com; 16192044@sun.ac.za; 17500966@sun.ac.za; coenrad@sun.ac.za).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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TABLE I
COMPONENT STAMPS FOR VOLTAGE

	LHS		RHS
R	$\begin{bmatrix} \frac{1}{R} & -\frac{1}{R} \\ -\frac{1}{R} & \frac{1}{R} \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \end{bmatrix}$		$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$
C	$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & -1 \\ 1 & -1 & \frac{h_n}{2C} \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \\ I_C \end{bmatrix}$		$\begin{bmatrix} 0 \\ 0 \\ -\frac{h_n}{2C} I_{n-1} - V_{n-1} \end{bmatrix}$
V	$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & -1 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \\ I_V \end{bmatrix}$		$\begin{bmatrix} 0 \\ 0 \\ V_n \end{bmatrix}$

where n is the iteration count and h_n the current time step in the transient analysis. This integration method is suitably accurate for circuit simulation purposes, however when a rapid change in y occurs such as a 2π Josephson phase switch, the derivative (voltage) tends to produce spikes.

A. Voltage

JoSIM programmatically creates component matrices using generic MNA stamps for the component type. We demonstrate the creation of these generic MNA stamps through an inductor as example.

$$v = L\frac{di}{dt} \tag{2}$$

If we apply the equation in (1) to (2) we obtain an equation for the inductor voltage that is dependent on the previous time step current and voltage.

$$V_n - \frac{2L}{h_n} I_n = -\frac{2L}{h_n} I_{n-1} - V_{n-1} \tag{3}$$

Where (3) can be written in general matrix form as

$$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & -1 \\ 1 & -1 & -\frac{2L}{h_n} \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \\ I \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ -\frac{2L}{h_n} I_{n-1} - V_{n-1} \end{bmatrix}$$

This general matrix form is used to solve the $Ax = b$ linear algebra problem in circuit simulation. The stamps for a resistor, inductor, capacitor and voltage source can be seen in Table I.

JoSIM uses the RCSJ model for which the MNA stamp coincides with the matrix found in JSIM, which relies on a second order guess of the phase for the next time step.

$$\begin{bmatrix} \frac{1}{R} + \frac{2C}{h_n} & -\frac{1}{R} - \frac{2C}{h_n} & 0 \\ -\frac{1}{R} - \frac{2C}{h_n} & \frac{1}{R} + \frac{2C}{h_n} & 0 \\ -\frac{h_n}{2}\frac{2e}{\hbar} & \frac{h_n}{2}\frac{2e}{\hbar} & 1 \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \\ \phi \end{bmatrix} = \begin{bmatrix} I_s \\ -I_s \\ \phi_{n-1} + \frac{h_n}{2}\frac{2e}{\hbar} V_{n-1} \end{bmatrix}$$

where the phase node ϕ is a virtual node not connected physically in the circuit and e and $\hbar$ are the electron charge and Plancks constant respectively.

$$I_s = -I_c \sin\phi^0 + \frac{2C}{h_n} V_{n-1} + C\dot{V}_{n-1} \tag{4}$$

TABLE II
COMPONENT STAMPS FOR PHASE

	LHS		RHS
R	$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & -1 \\ 1 & -1 & -\frac{\pi h_n R}{\Phi_0} \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \\ I_R \end{bmatrix}$		$\begin{bmatrix} 0 \\ 0 \\ \frac{\pi h_n R}{\Phi_0} I_{n-1} + \phi_{n-1} \end{bmatrix}$
L	$\begin{bmatrix} \frac{\Phi_0}{2\pi L} & -\frac{\Phi_0}{2\pi L} \\ -\frac{\Phi_0}{2\pi L} & \frac{\Phi_0}{2\pi L} \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \end{bmatrix}$		$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$
C	$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & -1 \\ 1 & -1 & -\frac{\pi h_n^2}{2C\Phi_0} \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \\ I_C \end{bmatrix}$		$\begin{bmatrix} 0 \\ 0 \\ \frac{\pi h_n^2}{2C\Phi_0} I_{n-1} + \phi_{n-1} + h_n\dot{\phi}_{n-1} \end{bmatrix}$
V	$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & -1 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \\ I_V \end{bmatrix}$		$\begin{bmatrix} 0 \\ 0 \\ \frac{\pi h_n}{\Phi_0}(V_n + V_{n-1}) + \phi_{n-1} \end{bmatrix}$

with

$$\phi_n^0 = \phi_{n-1} + \frac{h_n}{2}\frac{2e}{\hbar}\left(V_{n-1} + v_n^0\right) \tag{5}$$

and

$$v_n^0 = V_{n-1} + h_n \dot{V}_{n-1} \tag{6}$$

This method of using the phase guess relies on a voltage guess and subsequently information about the previous two values of the junction voltage as well as their derivatives. It is therefore necessary to keep track of these values throughout the transient simulation.

B. Phase

PSCAN, first introduced in 1991 utilized a similar method of computing the phase as standard variables, however this tool was practically unobtainable until s recent re-release by Shevchenko, written in Python, made it open-source (PSCAN2) [11]. The tool utilizes its own unique input language, SFQHDL, which allows the self-verification of circuit results using the built-in optimization engine.

The JJ is a phase-based element, therefore the direct calculation of the phase is more practical. It therefore becomes sensible to perform the entire transient analysis in phase since each component affects the phase of the entire circuit.

Calculation of phase is done through the Josephson voltage-phase relation [12], which is shown in (7). This relation can be substituted into every voltage dependent equation and expanded using the trapezoidal rule. This allows us to create modified nodal phase analysis (MNPA) stamps for each component. We provide these MNPA stamps in Table II for comparison.

$$v = \frac{\Phi_0}{2\pi}\frac{d\phi}{dt} \tag{7}$$

The JJ MNPA stamp remains mostly the same with simply the role of the voltage and phase swapped. This means that the phase is now the connected node which we want to calculate, and the voltage becomes a virtual non-connected node which is

required only for calculation purposes.

$$\begin{bmatrix} 0 & 0 & \frac{1}{R}+\frac{2C}{h_n} \\ 0 & 0 & -\frac{1}{R}-\frac{2C}{h_n} \\ 1 & -1 & -\frac{h_n}{2}\frac{2e}{\hbar} \end{bmatrix} \begin{bmatrix} \phi^+ \\ \phi^- \\ V \end{bmatrix} = \begin{bmatrix} I_s \\ -I_s \\ \phi_{n-1}+\frac{h_n}{2}\frac{2e}{\hbar}V_{n-1} \end{bmatrix}$$

The phase for the next time step remains the same second order guess as in (5) which utilizes a voltage guess as in (6).

Direct calculation of the phase allows the addition of DC external magnetic fields through mutual coupling with all the inductors in the circuit. This is a rather important feature in low temperature superconductivity due to the high susceptibility to external fields [13] which is not trivial using voltage-based methods.

III. JoSIM Features

JoSIM is written to accommodate standard SPICE syntax as well as the limited SPICE syntax utilized by JSIM. This allows the results of simulations to be quite easily compared with that of JSIM and WRspice. In addition to the capability to perform phase-based simulations, JoSIM provides other functionality that JSIM does not such as alpha-numeric node numbers.

The inclusion of an expression parsing algorithm based on Dijkstras shunting yard [14], with which variables can be generated within the SPICE netlist allows scaling, computation or parameterization of component values within the netlist.

JoSIM allows the output of result vectors in various ways including space- or comma-separated files. A key feature that is provided with JoSIM is the ability to plot the result vectors through either the cross-platform FLTK graphical library or the Python based matplotlib interface. The latter provides the ability to scale, label and save the results as publication grade figures.

IV. Test Methodology and Results

A. Test Methodology

We compare the quasiparticle resistance model used in JoSIM to the others. This is done by comparing the I-V curves which are generated by steadily ramping up the input current of a JJ, keeping it constant and averaging the voltage across the junction once stabilized. The current is incremented and the process is repeated until the input current reaches some large value whereafter the current is swept through zero to the negative peak and back to zero. Plotting these averaged voltage values against the current produces the I-V curve of the junction.

The only quasiparticle resistance models (Rtype) that are implemented in JoSIM at present is the zero shunt conductance (Rtype=0) and PWL resistance model (Rtype=1). This is similar to that found in JSIM, where WRspice has an exponentially derived resistance curve (Rtype=2), a fifth order polynomial expansion (Rtype=3) and a temperature variation model (Rtype=4) controlled by a specified voltage source or inductor. The models implemented by WRspice are scheduled for incorporation into JoSIM in the near future.

Additional tests are performed which benchmark the speed and simulation size capabilities of JoSIM compared to others. These benchmarks include a basic Josephson transmission line (JTL), a 4-bit Kogge-Stone Adder (4-bit KSA) and various large simulations created by stringing together JTLs up to a total of 10,000 JJs.

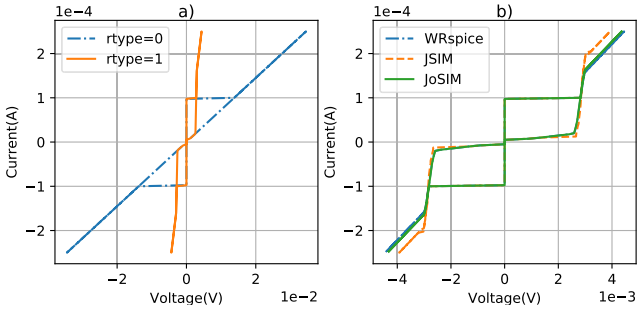

Fig. 1. a) JoSIM Rtype=0 and Rtype=1 I-V curves. b) JoSIM, JSIM, and WRspice Rtype=1 I-V curves.

B. I-V Curves

The first test involving the I-V curves of the JJ in JoSIM is presented in Figure 1a. The comparison between the I-V curve of JoSIM, JSIM and WRspice can be seen in Figure 1b. Since the JJ model used in JoSIM matches the one found in WRspice they are very close with the difference forming as a result of the way JoSIM approximates the voltage guess for the next time step.

The model used in JSIM differs from JoSIM and WRspice in the way the transitional current and conductance is calculated. JSIM approximates a transition conductance as the slope between the sub-gap and normal resistances for the gap voltage spread region (ΔV). Based on where the voltage is guessed to be in the next time step, the A matrix is adjusted using either sub-gap, transition or normal conductance. During the transitional state, two regions are defined namely $V_{gap}+\Delta V$ and $V_{gap}+2\Delta V$. When in the first region a constant current is added to the b matrix entry for the junction, where a varying current is added during the second region.

This model differs quite significantly from the one used in JoSIM and WRspice, where a single region ΔV is defined surrounding the gap voltage. The transition conductance is calculated using the critical current, ΔV and a ratio of critical to gap current (typically $\pi/4$). Similar to JSIM the A matrix is adjusted with the transitional conductance when entering the transition region, however the current with which the b matrix entry is adjusted differs and is continually added even when entering the normal resistive state.

This difference in RCSJ model implementation is what causes the normal region of WRspice and JoSIM to differ slightly when compared to JSIM. From internal data under the SuperTools project, we find that the WRspice/JoSIM JJ model provides a better match to measured I-V curves for the MIT Lincoln Laboratory SFQ5ee process [15].

C. JTL

The example tested using JoSIM is the basic JTL and is seen in Figure 2. We further compare these results to the same simulation performed using JSIM as well as WRspice and plot the percentage difference between the junction output phases. The

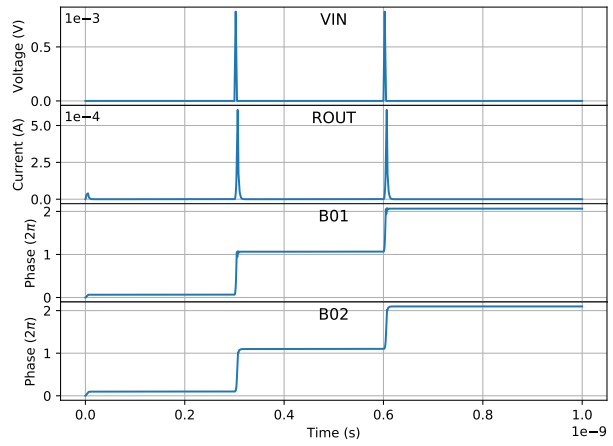

Fig. 2. Josephson transmission line (JTL) simulation using JoSIM.

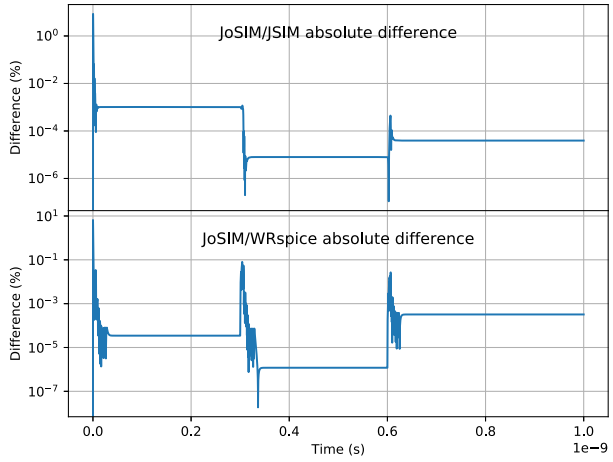

Fig. 3. JTL phase difference of JoSIM vs. JSIM and WRspice.

results of this comparison can be observed in Figure 3. The difference percentage scale is expressed in logarithmic form for greater clarity. The results are as expected with absolute differences between simulators less than a fraction of a percentage.

D. Execution Speed

The execution speed and simulation size capabilities of JoSIM were tested and compared to that of JSIM and WRspice. Each example is simulated with a time step of 0.25 ps with the maximum time step set to the same for a total of 1000 ps. The examples were executed on a system with an Intel Core i5 and 8GB RAM running macOS Mojave. The *time* command was used to measure the execution in seconds and each simulator was instructed to print results to a file. All examples, excluding the I-V curve, can be obtained on the online repository [17]. The results of these simulations are shown in Table III. In small examples simulators are quite closely matched however as the size of simulation grows JoSIM starts to gain ground, which is a good step towards VLSI simulation of superconducting circuits.

E. Phase Simulations

When performing phase-based simulations the phase of each node in the circuit is calculated. This method was implemented

TABLE III
COMPARISON OF SIMULATOR EXECUTION SPEEDS

Simulation		Execution times(s)		
Circuit Description	JJ Count	JSIM	WRspice	JoSIM
Basic JTL	2	0.057	0.107	0.134
400 simulation I-V curve	400	60.500	56.000	54.870
4-bit KSA	2,095	48.500	DNF	23.490
General Partial Products	3,904	93.000	64.000	20.900
3,000 JTL string	6,006	276.000	159.000	91.880
4,000 JTL string	8,006	>3,600.000	232.700	130.870
5,000 JTL string	10,006	DNF	263.800	169.810

*DNF: Did not finish. Non-convergence, time step too small

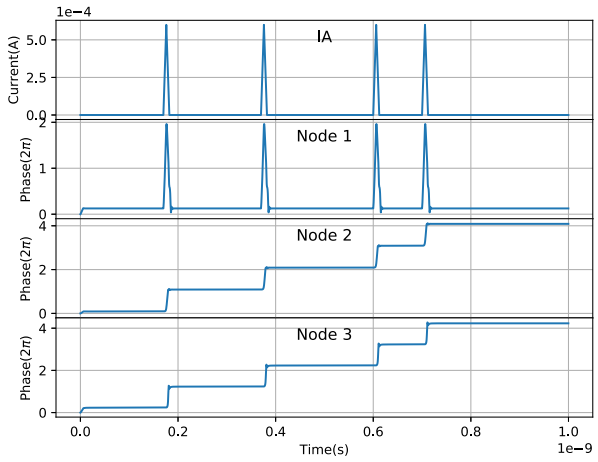

Fig. 4. Nodal phase analysis of a DC to SFQ connected to JTL with resistor termination.

in JoSIM in such a way that no alterations need be made to a circuit netlist to allow for phase-based analysis. We plot the results of the nodal phases of a DC to SFQ converter connected to a JTL and terminated using a resistor in Figure 4.

V. CONCLUSION

A superconducting circuit simulator JoSIM was demonstrated to have superior execution speed while maintaining accuracy. Voltage- and phase-based analysis methods were discussed in detail with demonstrations of each. The simulator was compared to popular existing alternatives as well as percentage difference measured.

JoSIM has been proven to be a reliable new superconducting circuit simulator with clear advantages in simulation speed as well as compatibility with multiple formats. Advanced features such as the capability to do both phase and voltage analysis, parameterize circuit netlists through expressions as well as natively plotting outputs and saving them in a variety of formats.

Development on this simulator will continue with efforts to introduce parallel processing in certain regions to further improve performance on large circuits being investigated. Additional RCSJ models are being considered for future releases along with the elusive microscopic tunnel junction [16].

Additional improvements planned for future implementation include the addition of noise to simulations as well as the modulation of temperature locally on a per component base, as well as globally across the circuit. Development can be tracked through the JoSIM open-source online repository [17].

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Appendix E

Journal Paper: Impedance Matching of Passive Transmission Line Receivers to Improve Reflections Between RSFQ Logic Cells

- L. Schindler, P. l. Roux and C. J. Fourie, "**Impedance Matching of Passive Transmission Line Receivers to Improve Reflections Between RSFQ Logic Cells**," in IEEE Transactions on Applied Superconductivity, vol. 30, no. 2, pp. 1-7, March 2020

The majority of the contributions to this article are from the co-authors. I contributed the margin optimization tool along with support for the tool that was used to optimize margins. IEEE Transactions on Applied Superconductivity hold the copyright for this article.

Impedance Matching of Passive Transmission Line Receivers to Improve Reflections Between RSFQ Logic Cells

Lieze Schindler, *Student Member, IEEE,* Paul le Roux, *Student Member, IEEE,* and Coenrad J. Fourie, *Senior Member, IEEE*

***Abstract*—Devices used for RSFQ cell interconnects include Passive Transmission Lines (PTLs) and Josephson Transmission Lines (JTLs). We demonstrate software analysis methods with which reflections on PTLs can be improved through impedance matching without compromising the margins of the connected RSFQ logic cells. RSFQ cells are typically designed to connect to PTL transmitters and receivers before attaching the PTL interconnects. These transmitters and receivers are used as matching and buffer stages between the cell and the PTL; and can be adjusted to minimize impedance mismatching. We integrate PTL transmitters and receivers within the RSFQ cell to decrease the amount of Josephson junctions required to incorporate PTL interconnect functionality. Frequency domain analysis on each cell provides equivalent impedance characteristics used for impedance matching.**

***Index Terms*—Circuit optimization, Impedance matching, Reflection coefficient, RSFQ, Superconducting integrated circuits**

I. Introduction

RAPID Single Flux Quantum (RSFQ) logic utilizes magnetic flux quanta passed between decision elements–which results in short voltage pulses as associated current passes through inductive connections–for data representation [1]. The quantized area of the voltage pulse, a few picoseconds wide, corresponds to a single flux quantum $\Phi_0 \approx 2.07 \times 10^{-15}$ Vs. These short SFQ pulses allow for high-speed digital applications with low power consumption. RSFQ cells can be connected directly using a non-storing inductive loop or, alternatively, the cells can be connected using Josephson Transmission Lines (JTLs) or Passive Transmission Lines (PTLs) [2]–[4] to bridge longer distances. The choice of cell connection depends on various factors. These include the required power consumption, transmission delay restrictions, available routing space on the chip, and distance between the two cells to be connected. JTLs can transmit pulses without reflections, but drawbacks include increased power consumption and higher probability of timing errors with increased JTL length due to jitter [5]. A major drawback of PTLs is pulse reflection due to an impedance mismatch between RSFQ cells and the PTL [6]. This can cause timing jitter and affect the operating margins of a circuit [7], [8]. A notable advantage of superconducting PTLs is high speed pulse propagation [9].

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The authors are with Stellenbosch University, Stellenbosch, South Africa (phone: +2721 808 4029; e-mail:17528283@sun.ac.za; 17500966@sun.ac.za; coenrad@sun.ac.za)

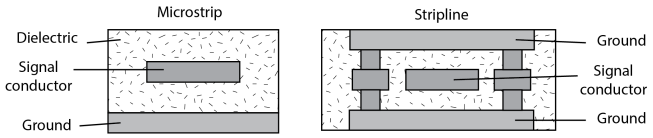

Fig. 1. Cross-section of typical thin-film passive transmission line geometries in superconductor integrated circuits for microstrip and stripline. The dielectric is mostly SiO2, layer thickness is in the range 100 to 500 nm, and line width is in the order of 5 to 10 μm.

Fig. 1 shows the typical structure of microstrip and stripline PTLs. In this work, we investigate a stripline PTL. Such a superconducting PTL, with a SiO_2 dielectric, typically has a phase velocity or pulse propagation speed of approximately $90-110$ μm/ps at 4.2 K (about $0.3c$), depending on the kinetic inductance contribution. For the MIT Lincoln Laboratory (MIT-LL) SFQ5ee fabrication process [10], a JTL with an approximate time delay of 5 ps can be laid out with a cell length of roughly 30 μm [11]. The JTL therefore has a pulse transmission of approximately 6 μm/ps. PTL interconnects thus allow signal transmission at more than an order of magnitude faster than JTLs [8].

In this article, we analyze methods for improving impedance mismatching focused towards application to the MIT-LL SFQ5ee fabrication process [10]. This research forms part of the ColdFlux project [12] under the IARPA SuperTools program [13]. For ColdFlux, placement-and-routing are developed that utilize PTLs for on-chip gate-to-gate interconnects [4], [14]. We therefore investigate how reflections induced by impedance mismatching between PTLs and transmitter/receiver cells can be improved, according to simulation, for the MIT-LL SFQ5ee fabrication process. We also analyze the influence of integrating the PTL transmitters and receivers within RSFQ cells and simulate these operating margins.

II. Impedance Matching, Noise and Margin Optimization

A. Pulse reflections

Pulse reflections are considered to be weak reflected waves which do not possess enough energy to switch a Josephson

junction (JJ) and are classified as weak noise [15]. These reflections are a result of impedance mismatch and can lead to a higher decision jitter [16]. If the circuit operates at its resonance frequency, the weak noise can accumulate on the PTL in such a way that it degrades the circuit's operating margins [6]. The resonance frequency is defined as:

$$f_{res} \equiv \frac{1}{T_{rt}}, \tag{1}$$

where T_{rt} is the round trip propagation time for a pulse through the PTL [15]. Optimal impedance matching for weak noise does not necessarily coincide with optimal impedance matching for SFQ pulse transmission. We shall focus on the theoretical impedance matching for weak noise and integrate the results into circuit improvement for SFQ pulse transmission.

B. Impedance matching

Impedance matching should also consider the physical constraints of a PTL stemming from chip layout. The width of a PTL can be adjusted to match the input impedance of the receiving cell, but factors like chip space, minimum PTL width and routing track pitch set firm constraints on this method of matching.

Impedance mismatch is often measured in terms of the reflection coefficient. The normalized reflection coefficient indicates the amount of pulse reflection on the PTL. Therefore, a small reflection coefficient indicates minimal impedance mismatch. The line's properties changes with frequency [17], and the reflection coefficient is therefore also dependent on frequency. At the operating temperature 4.2 K, and below the gap frequency, 750 GHz, the frequency-dependent effect can be ignored. The reflection coefficient can be approximated as:

$$\Gamma = \left| \frac{X_{in} - (X_o + Z_0)}{X_{in} + (X_o + Z_0)} \right|, \tag{2}$$

where X_{in} is the input impedance of the PTL receiver, X_o is the output impedance of the PTL transmitter and Z_0 is the characteristic impedance of the PTL at DC conditions. These definitions are discussed in Section III through Fig. 3 and 4 and (9) and (10).

The method of adjusting the characteristics of the PTL transmitters and receivers to match the impedance of the PTL is extensively discussed in [6], [15], [16], [18], [19]. We will follow a similar method, but will also investigate how this theory can be applied to integrate PTL transmitters and receivers within a RSFQ cell designed for the MIT-LL SFQ5ee fabrication process. Additionally, we analyze the characteristic impedance of a PTL designed for the MIT-LL SFQ5ee process and investigate how the margin optimization of the PTL transmitter and receiver circuits affect the SFQ pulse reflections on the PTL.

C. Margin optimization

The maximum amount of power is transferred when the least amount of pulse reflection occurs. This point of maximum power transfer should, theoretically, correspond to the operation point with optimal margins under the condition that the pulse reflections are dissipated before the next pulse arrives. We optimize the circuit margins by maximizing the statistical distance between the point of operation and all known points of failure. The maximization is achieved by repeatedly performing a margin analysis and, given the new information, stochastically searching for a new best point until convergence is reached. Many methods are discussed in the literature [20]–[23] and any optimization method leading to optimal margins should lead to sufficient results.

D. Vias and corners

In a placed and routed chip for very large scale integration, there are corners and vias along the length of a PTL in order to connect different cells. This is also used to implement PTL crossover. These corners and vias create impedance mismatch effects. These effects have to be investigated with a numerical model. The frequency dependence of the superconducting material properties and high-frequency reflection effects have to be taken into account in the numerical model. To our knowledge, this has not been done for superconductor integrated circuit thin-film passive transmission lines and is outside the scope of this paper.

If an equivalent model of the vias and corners can be simulated in SPICE, the netlist can be optimized with these effects included. The method of minimizing reflections using margin analysis presented here does not lose generality by not investigating the effects of corners and vias in our investigation.

III. Circuit Model Design

A. Josephson Junction

The Josephson Junction (JJ) is a non-linear device which can be approximated through various models. These include the Resistively and Capacitively Shunted Junction (RCSJ), the Nonlinear Resistively Shunted Junction (RSJN), the Tunnel-Junction-Microscopic (TJM) model, and variations of the above-mentioned models [24]. For our application, we chose the RCSJ model developed by [25] as the model is sufficient for critically damped superconductor-insulator-superconductor (SIS) tunnel junctions such as those used in the MIT-LL SFQ5ee process.

Fig. 2 shows the RCSJ model, as described in [24]. The model describes a Josephson impedance, X_{L}, in parallel with the internal capacitance, C_{J}, and the normal resistance, R_N. The model is extended with an external shunt resistor, R_{S}, and parasitic inductance L_{P}. The circuit symbol used to represent our extended RCSJ model is also shown in Fig. 2. The ideal Josephson inductance describes the characteristics at low frequencies and is defined as:

$$L_{\mathrm{J}} = \frac{\Phi_0}{2\pi I_{\mathrm{C}} \cos\phi}, \tag{3}$$

where I_c is the JJ critical current and ϕ is the Josephson phase [24]. We assume a constant biasing current, $I_b = I_c \sin\phi$, is applied and that $\sin\phi < 1$. The equivalent Josephson impedance at low frequencies is therefore:

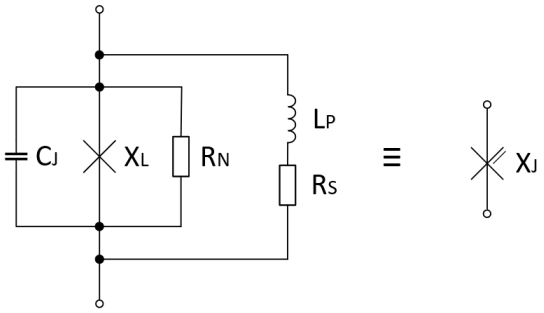

Fig. 2. Resistively and Capacitively Shunted Junction model with external shunt resistor, R_S, and parasitic inductance, L_P. The equivalent circuit symbol is shown on the right.

$$X_{\mathrm{L}} = j\omega L_{\mathrm{J}} = \frac{j\omega\Phi_0}{2\pi I_{\mathrm{C}}\cos\left(\arcsin\left(I_b/I_c\right)\right)}. \tag{4}$$

The equivalent impedance of the RCSJ model, X_J, in terms of frequency, ω, is described through the following equation:

$$X_{\mathrm{J}} = \left(\frac{1}{j\omega C_{\mathrm{J}}} \parallel X_{\mathrm{L}} \parallel R_{\mathrm{N}}\right) \parallel \left(j\omega L_{\mathrm{P}} + R_{\mathrm{S}}\right). \tag{5}$$

The model equation in (5) can be simplified under the following conditions [24, eq. (2.21)]:

$$R_{\mathrm{S}} \ll R_{\mathrm{N}} \quad \text{and} \quad \omega L_{\mathrm{p}} \ll R_{\mathrm{S}}; \tag{6}$$

where ω indicates the frequencies of interest, which for our purposes are well below the plasma frequency. We analyze at $f = 165$ GHz (to replicate [19]) and $L_{\mathrm{p}} \approx 1$ pH/□ if $R_{\mathrm{S}} \approx 2\ \Omega/\square$. The MIT-LL SFQ5ee fabrication process leads to a relatively large parasitic inductances caused by the external shunt resistor. As a result, the conditions in (6) are not met for the MIT-LL SFQ5ee process. The simplified model, as used in [15], [16], [18], [19], can therefore not be implemented in our case.

B. Passive Transmission Line

The width of a PTL influences the minimum track pitch of a circuit. A circuit utilizing a small track pitch can be laid out in a more compact format than a circuit with a larger track pitch. The assumption for a PTL with no loss and no dispersion can be made if the PTL length is $1 - 10$ cm [26]. We assume that all on-chip PTL connections will not exceed twice the chip side length – which is comfortable below 10 cm. The PTL model is therefore based on the assumption of a lossless PTL with the characteristic impedance defined as:

$$Z_0 = \sqrt{\frac{L_k + L_m}{C}}, \tag{7}$$

where L_k is the kinetic inductance, L_m is the magnetic inductance and C is the capacitance. As the width of the PTL is decreased, the capacitance decreases and the kinetic inductance increases. The change in magnetic inductance is neglectable for our purpose. Therefore, if the width of the PTL decreases, the characteristic impedance will increase.

The MIT-LL SFQ5ee fabrication process specifications were followed to design an example PTL layout with minimum width. Following this, a 4.5 μm superconducting stripline layout model was constructed. Using InductEx [27], along with the method discussed in [17], the characteristic impedance of the PTL was extracted as approximately 5 Ω. Similar theoretical results were calculated using the superconducting microstrip line characteristic impedance equation developed in [28].

The PTL cell connection is simulated in JoSIM [29] as a lossless transmission line with a characteristic impedance of 5 Ω. A transmission delay of 10 ps is selected (equivalent to a line length of about 1 mm). According to (1), the resonance frequency of the selected PTL will be:

$$f_{\mathrm{res}} = \frac{1}{T_{rt}} = \frac{1}{2 \cdot 10\ \mathrm{ps}} = 50\ \mathrm{GHz}. \tag{8}$$

We will therefore simulate a 50 GHz input pulse train connected to the PTL to analyze circuit behavior at the resonance frequency.

C. PTL transmitter and receiver

PTL transmitter circuits are used to transfer an SFQ pulse from an RSFQ circuit to a PTL and PTL receiver circuits reconstructs an SFQ pulse from the PTL to the RSFQ circuit. A JTL will act as a buffer as well as an SFQ pulse reconstruction device if it consists of two or more stages [18]. Fig. 3 shows how the PTL transmitter is designed as a two-stage JTL. The addition of a series resistor to either the transmitter or receiver circuit prevents flux trapping on the PTL along with providing improved impedance matching for weak noise [15], [30]. However, these series resistors also lead to unwanted attenuation of the SFQ pulse. The trade-off between improved impedance matching for weak noise and improved SFQ pulse transmission implementing these series resistors was analyzed in [15]; it was found that the resistor value can be optimized according to the characteristic impedance of the relative PTL. This was done through analyzing the effect of the series resistor when operating at resonance frequency and tuning the value of the resistor until a sufficient relation between SFQ pulse transmission and degree of pulse reflection was achieved.

Following the results of [15], we implement a series resistor of 1.36 Ω in the transmitter circuit, illustrated in Fig. 3. Implementing frequency domain analysis for weak noise, we derive the equation for the output impedance in Fig. 3 as:

$$X_{\mathrm{o}} = \left(X_{\mathrm{J1}} + j\omega L_2\right) \parallel X_{\mathrm{J2}} + j\omega L_3 + R. \tag{9}$$

A design similar to the PTL transmitter is used for the PTL receiver circuit. Fig. 4 shows the PTL receiver designed as a three stage JTL. The input impedance for the receiver circuit is calculated through:

$$X_{\mathrm{in}} = \left[\left(X_{\mathrm{J3}} + j\omega L_3\right) \parallel X_{\mathrm{J2}} + j\omega L_2\right] \parallel X_{\mathrm{J1}} + j\omega L_1. \tag{10}$$

The physical layout of transmitter and receiver circuits can cause major area overhead. Circuits implementing PTL connections can consequently require more chip area than

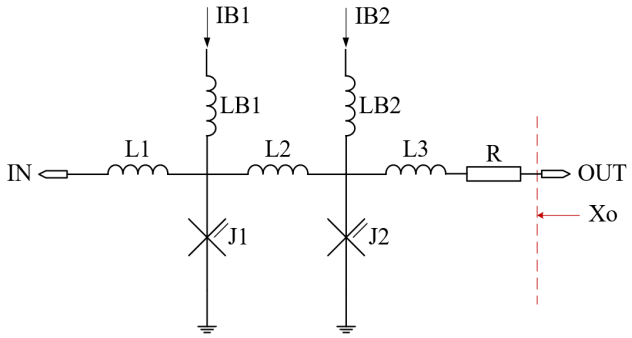

Fig. 3. Schematic of the designed PTL transmitter circuit. J1=200 μA, J2=162 μA, L1=2.5 pH, L2=3.3 pH, L3=2 pH and R=1.36 Ω.

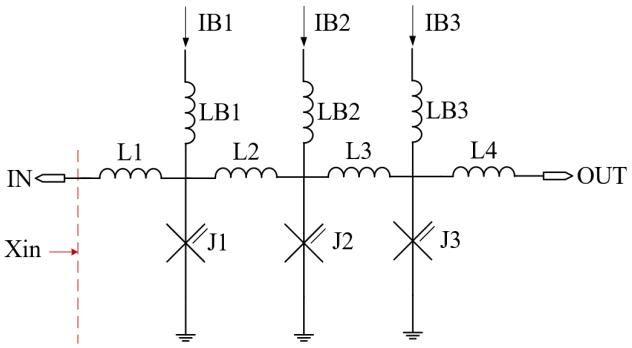

Fig. 4. Schematic of the designed PTL receiver circuit. J1=J2=150 μA, J3=250 μA, L1=2 pH, L2=4 pH, L3=4.2 pH and L4=2.8 pH.

circuits with conventional JTL connections [8]. We therefore integrate PTL transmitters and receivers within individual logic cells, as proposed in [31], for the ColdFlux project. Matching JJs can be removed through this integration, allowing the circuit area to be minimized.

IV. Simulation Results

A. Simulation setup

The MIT-LL process implements Nb/Al-AlOx/Nb Josephson junctions with a critical current density of 100 μA/μm^2 [10]. We set the McCumber parameter to $\beta_c \approx 1$ for all junctions to analyze a critically damped system. A lossless PTL with a characteristic impedance $Z_0 = 5\ \Omega$ is selected for simulation when a nominal critical current $I_{\text{Cnominal}} = 250\ \mu A$ is used. The biasing current is designed $I_b \approx 0.7 I_c$. This relation is known to produce minimal pulse reflections [6]. The parasitic inductances found within the physical cell layout is taken into consideration during the simulation.

The RSFQ cells were simulated in JoSIM [29] using the test circuit shown in Fig. 5. The source, typically a DCSFQ converter, is connected to a PTL transmitter (TX) followed by a PTL (Z_0) linked to the Device-Under-Test (DUT). The PTL receiver is integrated within the DUT together with the corresponding PTL transmitter. The current through the sink is measured to ensure the output pulse generated by the DUT

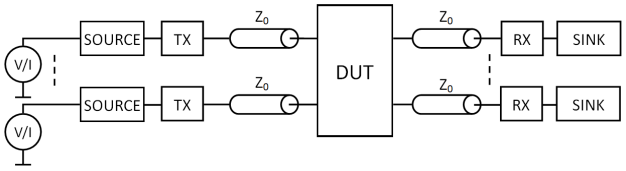

Fig. 5. Test circuit used for RSFQ circuit simulation. The Device-Under-Test (DUT) has integrated PTL transmitters and receivers.

retains enough energy to propagate through a PTL and switch the PTL receiver (RX).

B. Test cases

We use the DFF (Delay Flip-flop) as an example DUT for the circuit improvement process. We implement the results from (8) and drive the DUT with a pulse train at the resonant frequency, 50 GHz. The resonance frequency is used to analyze how the pulse reflections affect the circuit functionality when the worst case occurs [6].

We investigate three test cases where the DUT is connected as seen in Fig. 5.

- The first test case is a benchmark test where no circuit parameter optimization is performed on the DUT.
- The second test case optimizes all the circuit parameters of the DUT for optimal circuit margins, theoretically corresponding to optimal SFQ pulse transmission.
- The third test case analyzes how the results from the second test case affects the pulse reflections on the PTL, and optimizes selected circuit parameters to maximize impedance matching for weak noise.

The test cases analyze the normalized reflection coefficient along with the margins of the global parameters at the resonant frequency. The global margins represent the respective fabrication tolerance for Josephson junctions, inductances and biasing currents.

C. Reflection coefficient

The theoretical reflection coefficient is calculated using (2). The output impedance of the PTL transmitter was calculated, using (9), as $X_o = 2.320 + j3.429\ \Omega$. The characteristic impedance of the PTL simulated as $Z_0 = 5\ \Omega$. The DUT was simulated and the normalized reflection coefficient for the simulation was compared to the calculated value. The simulated area of the pulse voltage was calculated in the centre of the incoming PTL to determine the pulse reflection, normalized to the area of the input pulse. The resulting input impedance for the receiver, along with the calculated and simulated reflection coefficient for each test case is listed in Table I. The input impedance for the receiver was calculated using the ideal case which attributes to the difference between the calculated and simulated reflection coefficient in Table I.

We found that the complete margin optimization in the second test case did not drastically improve the simulated reflection coefficient. The receiver circuit in Fig. 4 is adapted for the third test case, according to results from [6], to adhere

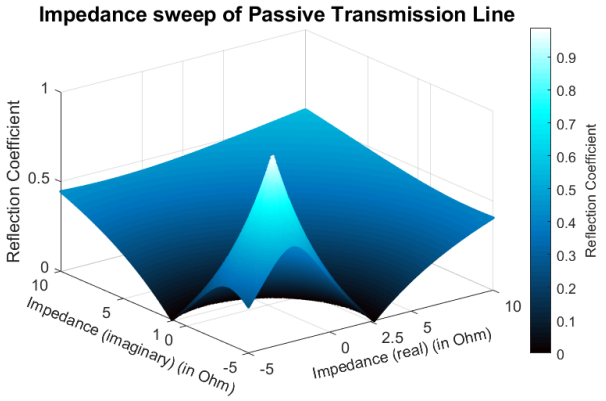

Fig. 6. Impedance sweep of a Passive Transmission Line investigating the Reflection Coefficient when connected to the designed RSFQ transmitter and receiver.

TABLE I
PARAMETER VALUES AND REFLECTION COEFFICIENT FOR RECEIVER CELL CONNECTED TO A 5 Ω PASSIVE TRANSMISSION LINE WITH DIFFERENT OPTIMIZATION METHODS

Optimization	Impedance (Ω)	Reflection Coefficient	
		Theoretical	Simulated
No optimization	1.621 + j3.410	0.3633	0.3597
Complete parameter	1.273 + j4.074	0.3089	0.3552
Selected parameter	1.191 + j5.125	0.2115	0.2395

to the inductance relation where both L_2 and $L_3 \approx \Phi_0/2I_c$. This relation provides constraints to the value of the PTL receiver input impedance to improve overall impedance matching with the PTL. Parameter value constraints are therefore placed on L_2 and L_3 during the second margin optimization process to investigate the resulting effect on the reflection coefficient. The results for the selected parameter optimization are listed in Table I and it is seen that the simulated reflection coefficient was reduced from 0.3597 in the first test case to 0.2395 in the third test case. The simulated reflection coefficient decreased by approximately 33% from test case one to test case three.

An impedance sweep of the PTL was done using MATLAB to determine the optimal operation point with a minimum reflection coefficient when the PTL is connected to the designed RSFQ PTL transmitter and receiver. The resulting graph is shown in Fig. 6. Negative impedances are shown on the graph, but are not viable implementation options. According to the impedance sweep, the optimal operation point for the PTL with minimum reflection will be at $Z_0 \approx 2.5\ \Omega$.

D. Global parameters

We also analyze the improvement in global parameter margins for each test case. These global parameter margins indicate the fabrication tolerances for Josephson junction values, inductance values and the biasing current of the circuit. A circuit with large operating margins for global parameter are more robust towards fabrication variations. The results are listed in Table II. It is seen that the margins are the most

TABLE II
GLOBAL PARAMETER MARGINS FOR A RECEIVER CELL CONNECTED TO A 5 Ω PASSIVE TRANSMISSION LINE

Optimization	Junctions		Inductance		Bias Current	
No optimization	-8.4	+16.2	-35.2	+51.3	-16.2	+12.0
Complete parameter	-15.5	+16.2	-50.6	+69.6	-21.8	+21.8
Selected parameter	-22.5	+15.5	-51.3	+75.9	-21.8	+26.7

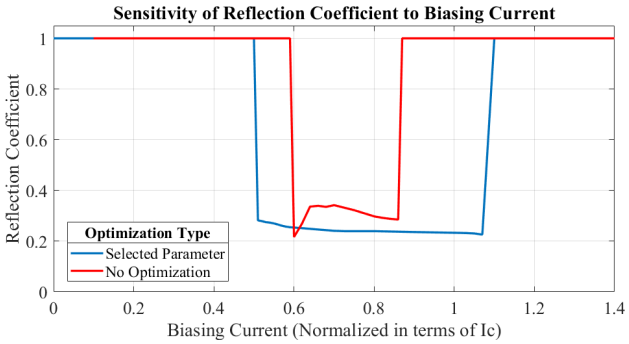

Fig. 7. Sensitivity of Reflection Coefficient to the biasing current for both the unoptimized and selected parameter optimized receiver circuits. The biasing current is normalized in terms of I_c. A reflection coefficient of 1 indicates a region of circuit malfunction.

improved for the selected parameter optimization. We deduce that the constraints placed on L_2 and L_3 leads to a more stable parameter optimization than the complete parameter optimization due to a more constant input impedance of the PTL receiver.

E. Influence of biasing current

The first test case designed the integrated PTL receiver and transmitter for $I_b \approx 0.7I_c$. This relation is known to produce minimal pulse reflections [6]. This relation is investigated through analyzing the sensitivity of the reflection coefficient at different values of I_b (for the receiver circuit) after the selected parameter optimization. The reflection coefficient is measured after a few pulses to ensure that the effects of the resonant frequency are present. Fig. 7 shows the comparison of the reflection coefficient of the circuit before optimization and after selected parameter optimization. A reflection coefficient of 1 indicates a region of circuit malfunction.

The reflection coefficient of the circuit with no optimization is more sensitive to the changes in biasing current than the case of selected parameter optimization. The minimum reflection coefficient, for the case of no optimization, is 0.2165 and is found at $0.6I_c$, which is on the edge of circuit malfunction. We found that, for the case of the DFF receiver circuit after selected parameter optimization, the reflection coefficient decreases slightly as I_b increases while $0.5I_c < I_b < 1.1I_c$. We deduce that the receiver circuit functions correctly at higher biasing currents, $1.0I_c \leq I_b < 1.1I_c$, due to current bleeding to the junctions within the DUT connected to the integrated PTL receiver circuit. The minimum reflection coefficient is 0.2262 and is found at $1.07I_c$, which is on the edge of circuit

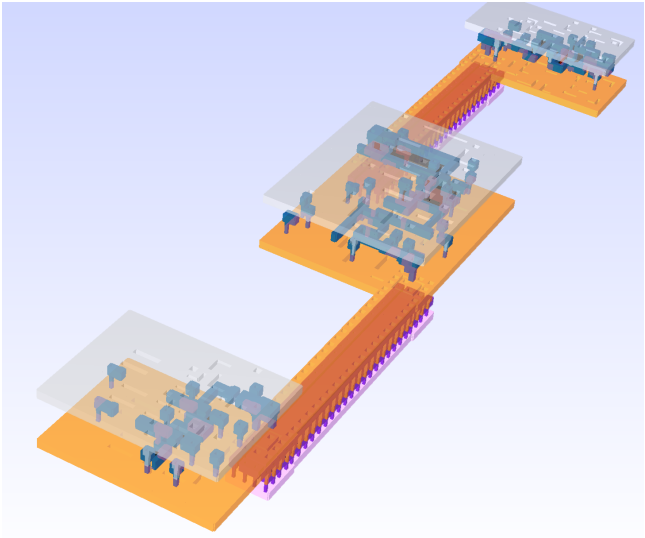

Fig. 8. Three-dimensional rendering of PTL test circuit to show the position of transmission lines below the ground plane in the MIT-LL SFQ5ee process. The vertical dimension has been stretched for clarity.

malfunction, similar to the case with no circuit parameter optimization.

V. Circuits

The PTL drivers and optimized receivers have now been implemented in the cells of the ColdFlux RSFQ cell library. A low-frequency test circuit was designed for fabrication in the MIT-LL SFQ5ee process [10], although the objective was to test magnetic rule checking models and tools as described elsewhere [32]. A three-dimensional rendering of the test circuit with InductEx is shown in Fig. 8. This test setup only verifies that the transmitter-PTL-receiver combination transmits SFQ pulses successfully, and cannot be used to measure reflection coefficients.

In future work, we will add high-frequency on-chip test structures to test the efficiency of the optimization.

VI. Conclusion

We investigated different methods to improve pulse reflections on PTLs. The PTL transmitter and receiver circuits were designed as JTLs to act as SFQ pulse reconstruction devices as well as a buffer between the stripline PTLs and connected cells for the MIT-LL SFQ5ee process. We investigated pulse reflections at resonance frequency and simulated the test circuit for the worst case scenario. The trade-off between circuit improvement for weak noise and the optimization for SFQ pulse transmission was analyzed. We found that the inductances within the PTL receiver circuit has a large influence in the reduction of pulse reflections. Constraints were placed on selected inductors during the optimization process. We were able to improve simulated pulse reflections for the DFF by approximately 33%. It was found that the pulse reflections after selected parameter optimization were minimally influenced by the bias current of the receiver circuit when the cell is within the operating region. The optimized PTL receiver circuits now form part of every cell with integrated PTL receivers in our ColdFlux RSFQ cell library.

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Appendix F

Journal Paper: Improved Transmission Line Parameter Calculation Through TCAD Process Modeling for Superconductor Integrated Circuit Interconnects

- H. F. Herbst, P. l. Roux, K. Jackman and C. J. Fourie, "**Improved Transmission Line Parameter Calculation Through TCAD Process Modeling for Superconductor Integrated Circuit Interconnects**," in IEEE Transactions on Applied Superconductivity, vol. 30, no. 7, pp. 1-4, Oct. 2020

The majority of the contributions to this article are from the co-authors. I contributed the PTL solver, which was used to extract the TCAD model parameters.

Improved Transmission Line Parameter Calculation Through TCAD Process Modeling for Superconductor Integrated Circuit Interconnects

Heinrich Frederick Herbst, Paul le Roux, *Student Member, IEEE*, Kyle Jackman, *Member, IEEE*, and Coenrad Johann Fourie, *Senior Member, IEEE*

***Abstract*—The Florida Object-Oriented Device, Process and Reliability Simulator (FLOOXS) technology computer-aided design process modeling tools developed at the University of Florida have been adapted under the Intelligence Advanced Research Projects Activity SuperTools program to support the MIT Lincoln Laboratory SFQ5ee fabrication process. We use FLOOXS to build meshed models of passive transmission lines from superconductor integrated circuit layouts. We have previously developed a numerical solver that extracts transmission line parameters from the meshed model. In this work, we convert a layout slice to FLOOXS inputs, generate two-dimensional meshes of cross-sectional geometries from simulated process steps, and then extract the transmission line parameters from the meshes. Results are shown compared against the results for simplified transmission lines that do not utilize process modeling. The results confirm that process modeling alters the extracted parameter values and suggest that process modeling will become more important as cell density of superconducting electronics increases. We conclude with a discussion on the necessity of process modeling for high-quality parameter extraction.**

***Index Terms*—Florida Object-Oriented Device, Process and Reliability Simulator (FLOOXS), passive transmission line, superconductor process modeling, technology computer-aided design (TCAD).**

I. Introduction

TECHNOLOGY computer-aided design (TCAD) is well-established for semiconductor processes. Modeling of the Josephson junction fabrication steps for superconductor electronics (SCE) requires the extension of existing TCAD tools. The University of Florida (UFL) is currently undertaking such a task with the active development of the Florida Object-Oriented Device, Process and Reliability Simulator (FLOOXS) [1]. Process modeling is required to determine accurate device geometry, stress profiles, electrical characteristics, and thermal effects, all of which are used to extract high fidelity simulation models of on-chip devices for circuit design and verification. Some of our work towards the ColdFlux project [2] under the Intelligence Advanced Research Projects Activity (IARPA) SuperTools program [3] includes the creation of a tool to aid in modeling the process of superconductor electronic fabrication, which uses FLOOXS as the simulation engine.

In this article, we briefly discuss FLOOXS, and then show a 2-D cross section of a passive transmission line (PTL). The cross section is processed in FLOOXS to generate a 2-D mesh, which is postprocessed before transmission line parameters are extracted with a numerical solver. We then analyze the original simplified model and compare the results of both to evaluate the influence of the new geometry profile. We repeat this process for models of identical layer thickness with varying widths.

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The authors are with the Stellenbosch University, Stellenbosch 7600, South Africa (e-mail: 18968708@sun.ac.za; 17500966@sun.ac.za; kjackman@sun.ac.za; coenrad@sun.ac.za).

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II. Florida Object-Oriented Process Simulator (FLOOPS)

The process modeling module of FLOOXS, FLOOPS, simulates how materials are deposited onto an integrated circuit (IC) die. FLOOPS achieves process simulation through the utilization of numerical methods such as the finite element method [1] and the level set method (LSM). The LSM tracks the movement of interfaces implicitly. FLOOPS uses the LSM to simulate the deposition and etching processes to construct a 2-D mesh of the cross section being analyzed. A bottom-up approach is followed in the same way that an integrated circuit is fabricated. The user supplies a script to FLOOXS in which information such as deposited material, deposition time and method, and other parameters are defined. Mask-based etching is also handled, but planarization is not yet supported. The simulator then performs functions, such as deposition and etching, in the sequence that they are defined in the script, after which FLOOXS produces a mesh of the required 2-D section.

III. Passive Transmission Line Models

A. Description of a PTL

A PTL is a strip of superconducting metal placed between circuit elements to connect them, allowing for ballistic pulse propagation in single flux quantum (SFQ) circuits. It is suitable

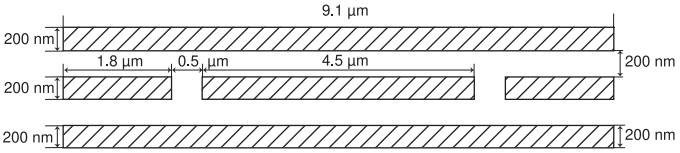

Fig. 1. Passive transmission line cross section.

TABLE I
EXTRACTED PER MODEL PTL PARAMETERS

Scale	Parameter	Approximate Model	Accurate Model	Percentage Error
0.25X	$C\ (nF \cdot m^{-1})$	0.6673	0.6619	-0.81
	$L\ (nH \cdot m^{-1})$	177.40	178.62	0.68
	$Z_0\ (\Omega)$	16.305	16.428	0.75
	γ	683.61	683.19	-0.06
	$I_{peak}\ (A \cdot m^{-2})$	375.68	410.35	8.45
0.50X	$C\ (nF \cdot m^{-1})$	1.064	1.066	0.16
	$L\ (nH \cdot m^{-1})$	100.49	100.79	0.30
	$Z_0\ (\Omega)$	9.717	9.724	0.07
	γ	649.79	651.27	0.23
	$I_{peak}\ (A \cdot m^{-2})$	339.44	369.79	8.21
0.75X	$C\ (nF \cdot m^{-1})$	1.511	1.523	0.79
	$L\ (nH \cdot m^{-1})$	69.72	69.81	0.13
	$Z_0\ (\Omega)$	6.793	6.770	-0.33
	γ	644.88	647.88	0.46
	$I_{peak}\ (A \cdot m^{-2})$	330.86	360.97	9.35
1.00X	$C\ (nF \cdot m^{-1})$	1.964	1.982	0.88
	$L\ (nH \cdot m^{-1})$	53.30	53.26	-0.09
	$Z_0\ (\Omega)$	5.209	5.184	-0.49
	γ	642.92	645.51	0.40
	$I_{peak}\ (A \cdot m^{-2})$	327.70	358.23	8.52
1.25X	$C\ (nF \cdot m^{-1})$	2.422	2.455	0.94
	$L\ (nH \cdot m^{-1})$	43.13	43.00	-0.30
	$Z_0\ (\Omega)$	4.220	4.194	-0.63
	γ	642.12	644.20	0.32
	$I_{peak}\ (A \cdot m^{-2})$	326.49	356.66	8.46
1.50X	$C\ (nF \cdot m^{-1})$	2.880	2.896	0.53
	$L\ (nH \cdot m^{-1})$	36.21	36.20	-0.01
	$Z_0\ (\Omega)$	3.546	3.536	-0.27
	γ	641.67	643.32	0.26
	$I_{peak}\ (A \cdot m^{-2})$	325.97	355.47	8.3

for modeling with FLOOXS as it is relatively simple, and we can make the simplifiying assumption that the physical properties do not vary along the length of the transmission line. The dimensions of the PTL designed for the MIT-LL SFQ5ee process [4] are shown in Fig. 1. This is the approximate model. Dimensions were chosen to correspond to published results [5].

B. Assumptions

We used the following assumptions for all PTL models. The PTL is infinitely long, perfectly symmetrical, and isotropic with no losses in the dielectric. The PTL solver [5] utilizes the two-fluid model to determine the complex capacitance $\hat{C}$ and complex inductance $\hat{L}$. No losses are assumed in the dielectric, so that both have only real components. The PTL solver also determines characteristic impedance Z_0, propagation constant γ, and maximum current density I_z of both the simplified and the process modeled PTLs. These parameters are, respectively, listed in Table I for each model. FLOOXS reveals that the physical profile of the passive transmission line layers differs from the rigid rectangular shape of the approximate model.

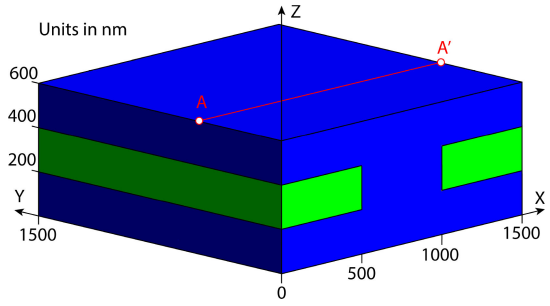

Fig. 2. Two layers of niobium connected by via through silicon dioxide.

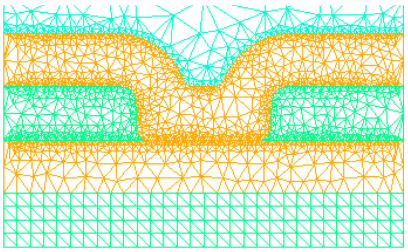

Fig. 3. Sample mesh output from Katana generated FLOOXS script.

IV. GEOMETRICAL MODELING

Process modeling is resource intensive. As such, a designer should be able to identify areas of a device or cell layout where process modeling is necessary. Through the combination of process layer information and geometrical descriptions of each layer, it is possible to describe the geometry of a cell fully.

We describe IC layouts in the Calma GDSII stream file format [6]. The GDS files only describe the layout masks, and thus, need to be used with process-specific information to derive the physical properties of an integrated circuit die. The designer must also be familiar with the design rules, materials, and layer properties of the fabrication process they are utilizing. The layer definition file (LDF) is a file specification created for use with Inductex [7], [8] that describes the mask and physical information for each layer of the fabrication process. Consequently, each fabrication process has its own associated LDF file.

We have created software (named Katana), which allows the generation of 2-D cross sections through cells. Katana accepts a GDS file, LDF file, and two co-ordinate pairs as an input. It analyzes each layer utilizing a combination of calculated points of interception and the winding number algorithm to solve the point-in-polygon problem to generate the 2-D cross-sectional layer segments. Katana then generates a FLOOXS process-modeling input script based on the cross section information, which greatly simplifies the modeling process. Gmsh [9] is used for meshing. Katana can also generate a cross section directly, omitting process modeling. A simple geometrical shape has been generated to illustrate how Katana works. Fig. 2 represents two layers of niobium connected through a layer of silicon dioxide by an etched via through the center. The user calls the cross section generation module of Katana by using the "Slice" command and specifying the GDS and LDF files and the cross section coordinates as parameters.The FLOOXS script is then processed by FLOOXS to generate the mesh shown in Fig. 3. Katana allows

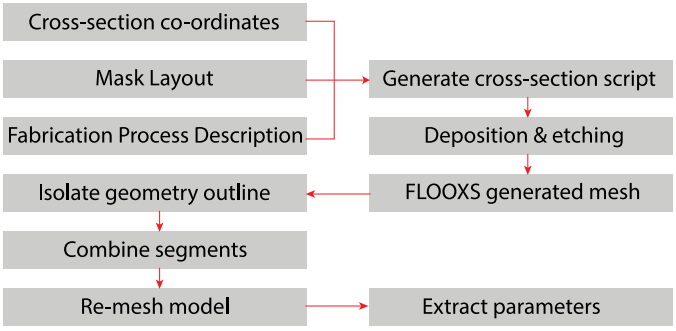

Fig. 4. Flow-chart of simulation process.

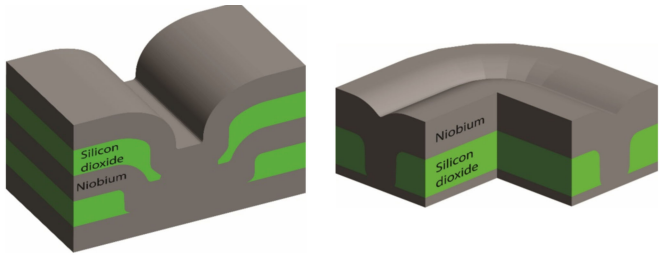

Fig. 5. Example 3-D process-modeled structures.

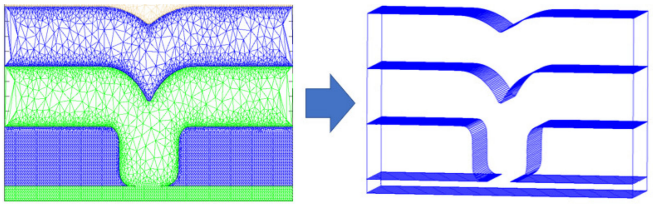

Fig. 6. Boundary identification and extrusion.

a designer to peer into multiple relevant areas of a cell quickly to aid in physical model construction.

V. Postprocessing

FLOOXS generates an unmodifiable mesh. Therefore, post-processing is required to allow mesh combination and extrusion. Our program converts FLOOXS-output mesh files into Gmsh geometry files (.geo). We optimize the mesh structure by reducing the number of nodes required to represent the mesh file. The program identifies layer boundaries to delimit cross-sectional objects and attributes the respective material layer properties to each such object. The outline of each layer's geometry is retained while the internal mesh structure is removed. The resulting geometry file can be remeshed and combined with other geometrical data to generate more complex structures. A flow-chart of the simulation process is shown in Fig. 4. The simulation process allows for simplified 3-D structures such as the examples in Fig. 5 to be created by extrusion or by a combination of separately oriented 2-D segments. Fig. 6 shows an example of the boundary identification and extrusion process of a multiple-layer cross section of niobium and silicon dioxide. We can combine multiple cross sections, where one is insufficient for simulating the complexity of a process. We retain control over the mesh to refine the complexity of the mesh in areas of interest.

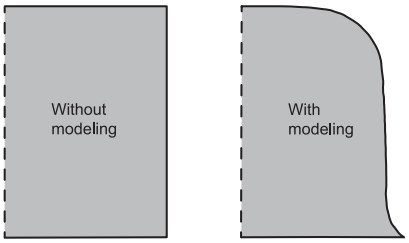

Fig. 7. PTL center strip edge before and after process modeling.

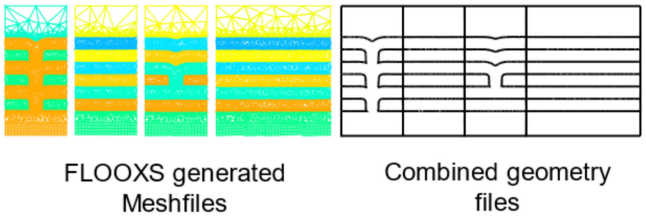

Fig. 8. Illustration of PTL mesh segment conversion and geometry combination.

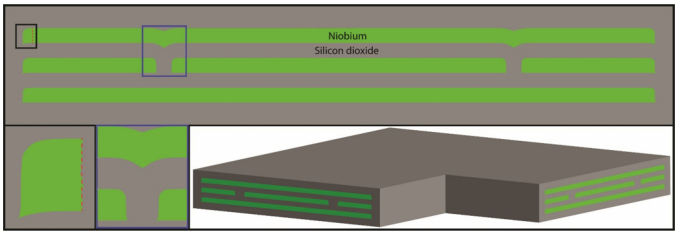

Fig. 9. Final passive transmission line cross-sectional model.

VI. Results

As a demonstration example, five pairs of PTL models were created with line widths scaled between 0.25 and 1.5 times the widths specified in Fig. 1. The objective is to determine how much of a role process modeling plays with regards to parameter extraction of a PTL. A close-up comparison between the edges of the simplified model and the process model, generated by FLOOXS, can be seen in Fig. 7. In order to reduce resource usage, four separate slices were made with Katana and the resulting FLOOXS meshes were combined programmatically, as shown in Fig. 8. The left half of the PTL was modeled and reflected about the PTL's vertical line of symmetry. The geometry of the final model can be seen in Fig 9. The warping and bow effects are emphasized in the zoomed rectangles. As all models assume the length of the passive transmission line is infinite, the 90° bend in Fig. 9 is purely illustrative. Fig. 10 shows the scaled current density of the accurate model. The simulation reveals an increased current density along the tip of the center conductor.

The extracted parameters for all five PTL models are listed in Table I. The absolute errors in parameters are calculated under the logical assumption that the TCAD-modeled PTL is closer to what the physical parameters would be.

All absolute error values approach zero as the width of the PTL increases. This is due do the edges of the PTL segments becoming less significant as the ratio of etched surface to flat

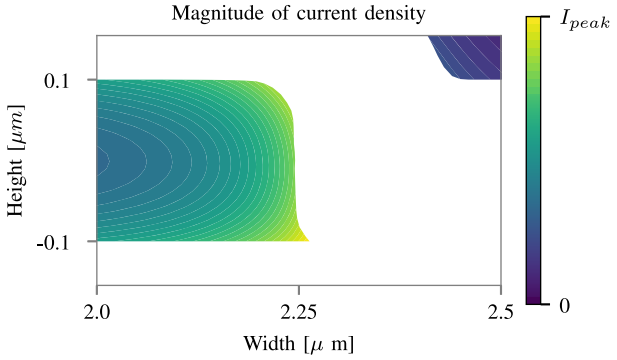

Fig. 10. Current density across center strip edge of 1.00X scale process-modeled PTL.

surface decreases. The etched edges of the niobium strip contribute a relatively small amount to the overall parameters in such a wide PTL. In a narrower transmission line, the ratio of curved to flat geometry is higher. Therefore, the error between models using the rectangular approximation and those which accurately model the etches will be more substantial. As discussed previously [5], when localized current density in the corners of the transmission line exceeds the critical current density, superconductivity ceases and current is redistributed. This effect is more pronounced when the conductor has sharp edges. The current crowding effect (CCE) is the change in the distribution of current caused by the tendency of current to flow through the least resistive path of a circuit [10]. While the CCE was initially observed in semiconductors, the effect applies to superconductors too [11]. It is expected that current crowding at the edges of the transmission line will first cause the current density in the sharp regions to exceed the critical current. However, instead of the strip heating, the current will redistribute so as not to exceed the critical current density, while maintaining superconductivity. For rapid single-flux-quantum (RSFQ) transmission lines, which transmit transient SFQ pulses, which are not strong enough to break superconductivity, current crowding at the edges of the transmission line can be neglected safely providing the designer follow the design rules specified for the fabrication process. The measured results are more likely to be pertinent when designing higher power transmission lines such as the ac clock/power lines used in adiabatic quantum-flux-parametron (AQFP) logic. AQFP circuits, such as the one used to demonstrate an AQFP-RSFQ interface [12] operate with clock currents in the mA range, compared to Josephson junction critical current densities, which lie in the order of μA.

VII. Conclusion

We have implemented a method to apply process modeling with FLOOXS to superconductor integrated circuits and applied it to the analysis of stripline PTL structures.

The PTL is one of the simplest SCE components. The Josephson junction, for which a process model is under development at the University of Florida [2], is more geometrically complex. Its parameters will deviate more than those of the PTL and process modeling will be substantially more important. Additionally, even slight differences in parameters can have a compounding effect when the circuit element forms part of a larger cell. Without process modeling, high-quality parameter extraction is difficult to achieve. As shown in the semiconductor industry, technology CAD is a vital stage in the cyclical and iterative process that is circuit design. As the density of superconductor electronics increases, cell sizes must be reduced. Cells will inevitably lie within closer proximity to each other. Because of the need for smaller cell elements, process geometry will play a more significant role in parameter extraction, and therefore, TCAD will become a necessity.

Currently, superconductor process modeling is limited to 2-D cases. This limitation means that models have to be built with some assumptions made and with reliance on symmetry and 1-D isotropic extrusion. Work is currently underway to develop a 3-D FLOOXS engine. Until such an engine is a reality, we can automate much of the process of creating a FLOOXS input script and extracting parameters from the resulting mesh with Katana.

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Appendix G

Vector Fitting Transforms

The vector fitting transform can be performed on a transformed problem, and the inverse transform used to get the desired model. Linear subtraction, differentiation, and integration will be covered.

All the transforms will start from the weighted fitting approximation, as shown in (G.1).

$$wH_{fit} \approx wH. \tag{G.1}$$

G.1 State Space subtraction

We want to reformulate the weighted fitting function with a known parallel system. We assume H_{fit} is the summation of an unknown system, $H_{fit}^{'}$ and a known system, H_{prior}. By subtracting the known system multiplied by the weight function from (G.1) we manipulate (G.1) into

$$wH_{fit}^{'} \approx w(H - H_{prior}). \tag{G.2}$$

The final state-space system can be constructed by adding the two in parallel. The state-space system is given by

$$s\mathbf{X}(s) = \begin{bmatrix} \mathbf{A}_{prior} & \mathbf{0} \\ \mathbf{0} & \mathbf{A} \end{bmatrix} \mathbf{X}(s) + \begin{bmatrix} \mathbf{B}_{prior} \\ \mathbf{B} \end{bmatrix} \mathbf{U}(s), \text{ and} \tag{G.3}$$

$$\mathbf{Y}(s) = \begin{bmatrix} \mathbf{C}_{prior} & \mathbf{C} \end{bmatrix} \mathbf{X}(s) + (\mathbf{D}_{prior} + \mathbf{D})\mathbf{U}(s). \tag{G.4}$$

G.2 State Space Integration

We want to reformulate the weighted fitting problem to enforce a pole at the origin. We assume H_{fit} has a pole at the origin and can be defined as $H_{fit} = \frac{H_{fit}^{'}}{s}$. By multiplying the right hand side of (G.1) with $1 = \frac{s}{s}$ we manipule (G.1) into

$$(\frac{w}{s})H_{fit}^{'} \approx (\frac{w}{s})sH. \tag{G.5}$$

Equation (G.5) corresponds to fitting the differentiated system. The integrated system can then be integrated to get the final system.

The integrated system can be constructed by cascading the system with a simple integrator system. The resulting state-space system is given by

$$s\mathbf{X}(s) = \begin{bmatrix} \mathbf{0} & \mathbf{0} \\ \mathbf{B} & \mathbf{A} \end{bmatrix} \mathbf{X}(s) + \begin{bmatrix} \mathbf{I} \\ \mathbf{0} \end{bmatrix} \mathbf{U}(s), \text{ and} \tag{G.6}$$

$$\mathbf{Y}(s) = \begin{bmatrix} \mathbf{D} & \mathbf{C} \end{bmatrix} \mathbf{X}(s). \tag{G.7}$$

G.3 State Space Differentiation

We want to reformulate the weighted fitting problem to enforce zeros at the origin. We assume H_{fit} has a zero at the origin and can be defined as $H_{fit} = sH_{fit}^{`}$. By multiplying the right hand side of (G.1) with $1 = \frac{s}{s}$ we manipule (G.1) into

$$(sw)H_{fit}^{`} \approx (sw)\frac{H}{s}. \tag{G.8}$$

Equation (G.8) corresponds to fitting the integrated system. The integrated system can then be differentiated to get the final system.

We, therefore, need to find the state space representation of a differentiated system. We start from the transfer function to derive the state space representation of a differentiated system.

$$\begin{aligned} \mathbf{H}(s) &= \mathbf{C}(s\mathbf{I} - \mathbf{A})\mathbf{B} + \mathbf{D} \\ \mathbf{h}(t) &= \mathbf{C}e^{\mathbf{A}t}\mathbf{B} + \mathbf{D}\delta(t) \\ \frac{d}{dt}\mathbf{h}(t) &= \mathbf{C}\mathbf{A}e^{\mathbf{A}t}\mathbf{B} + \frac{d}{dt}\mathbf{D}\delta(t) \\ s\mathbf{H}(s) - \mathbf{h}(0^+) &= \mathbf{C}\mathbf{A}(s\mathbf{I} - \mathbf{A})\mathbf{B} + s\mathbf{D} - \mathbf{D}\delta(0^+) \\ s\mathbf{H}(s) &= \mathbf{C}\mathbf{A}(s\mathbf{I} - \mathbf{A})\mathbf{B} + \mathbf{C}\mathbf{B} + s\mathbf{D} \end{aligned} \tag{G.9}$$

We now have everything we need to implement a program that can determine a PTL model while enforcing modal accuracy.

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